A1+ Block Diagram

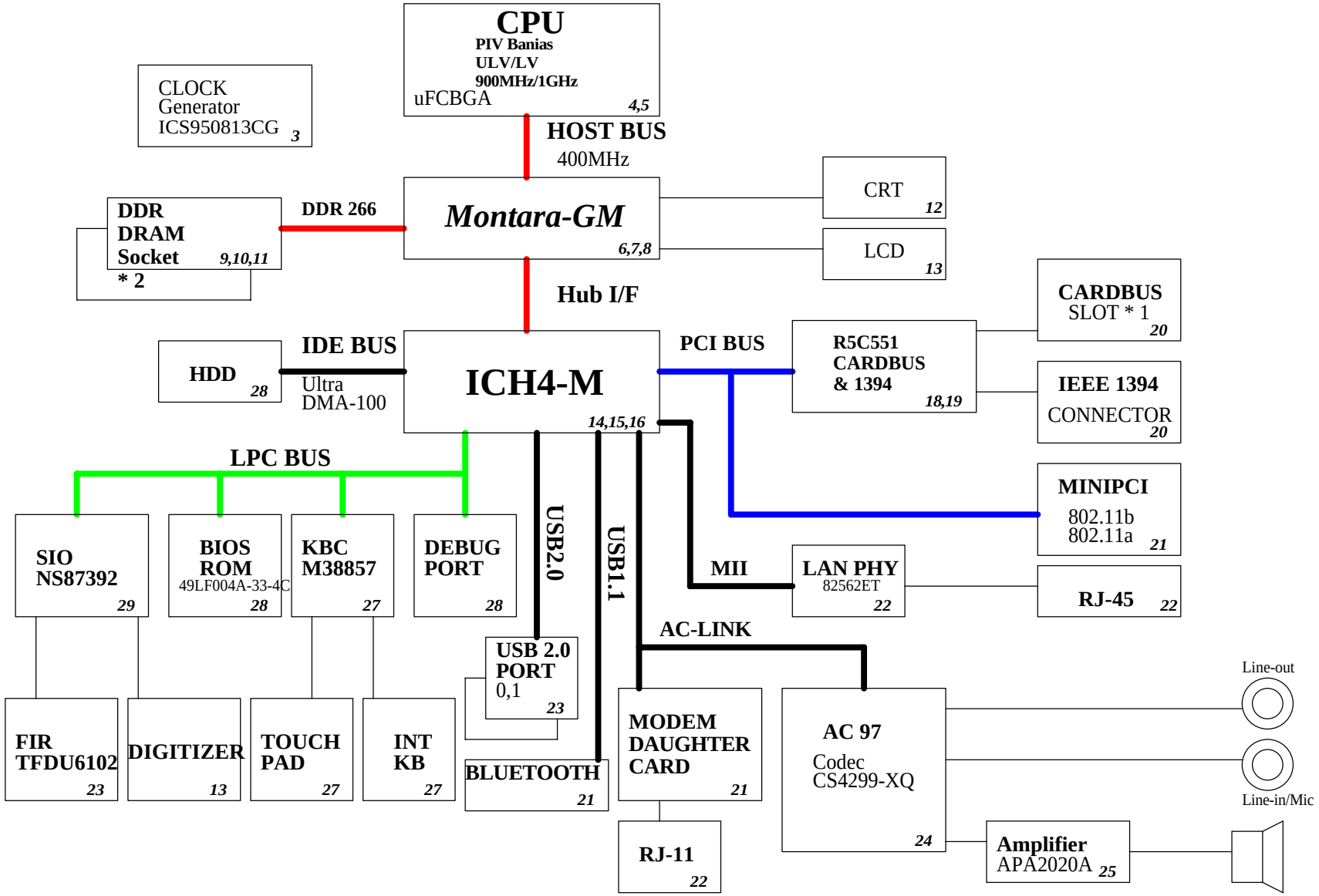
DC/DC IMVP4 Switching Power Max1907AETL 32	
INPUTS	OUTPUT
DCBATOUT	VCC_CORE

1.2/1.05V DC/DC TPS5110 33	
INPUTS	OUTPUTS
DCBATOUT	1D2V_S0 1D05V_S0

DC/DC&CHARGER Max1645 36	
INPUTS	OUTPUTS
AD+	BT+

3V/5V/2D5V/1D8V DC/DC TPS5130 35	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5 2D5V_S3 1D8D_S0

CM8500/APL1805 34	
INPUTS	OUTPUTS
2D5V_S3 3D3V_S5	1D25V_DC_S0 1D5V_DC_S0



Port Replicator (100 PIN)

AC IN | RJ11 | RJ45 | SEARIAL PORT | CRT | PRINTER | USB*2 | PS2 | MIC | LINE IN | LINE OUT

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Title: BLOCK DIAGRAM

Size: A3 | Document Number: A1+ | Rev: -1

Date: Monday, March 03, 2003 | Sheet 1 of 39

A1+ PCI Routing Table ver. 0.1

DEVICE	IDSEL	IRQ	DREQ/DGNT
R5C551	AD17	A/D	REQ0#/GNT#0
Mini PCI	AD21	B/C	REQ3#/GNT#3

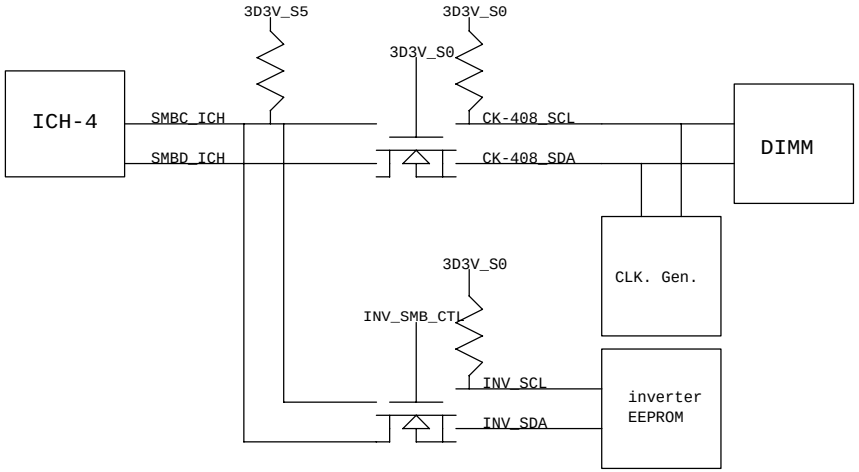
N/B H/W TRAP

Pin Name	Strap Description	Configuration	I/F Type Buffer Type
LCLKCTLB	CPU Strap	Low=Banias processor (default)	GPIO
GST(1) GST(0)	Clock Config:Bit_1 Clock Config:Bit_0	**Key:PSB/Sys Mem Core/GFX Core/(CL/CH(Core Clock)): 00(def)=Config#0 (400/266/200/(133/200)) 01=Config#1 (400/200/200/(100/200)) 10=Config#2 (400/200/133/(100/133))**	**DVO**

WOL & WOR

WOL

	AC Adaptor	Battery Only
S1	Can	Can
S3	Can	No
S4	Can	No
S5	Can	No



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Title: REVISION HISTORY

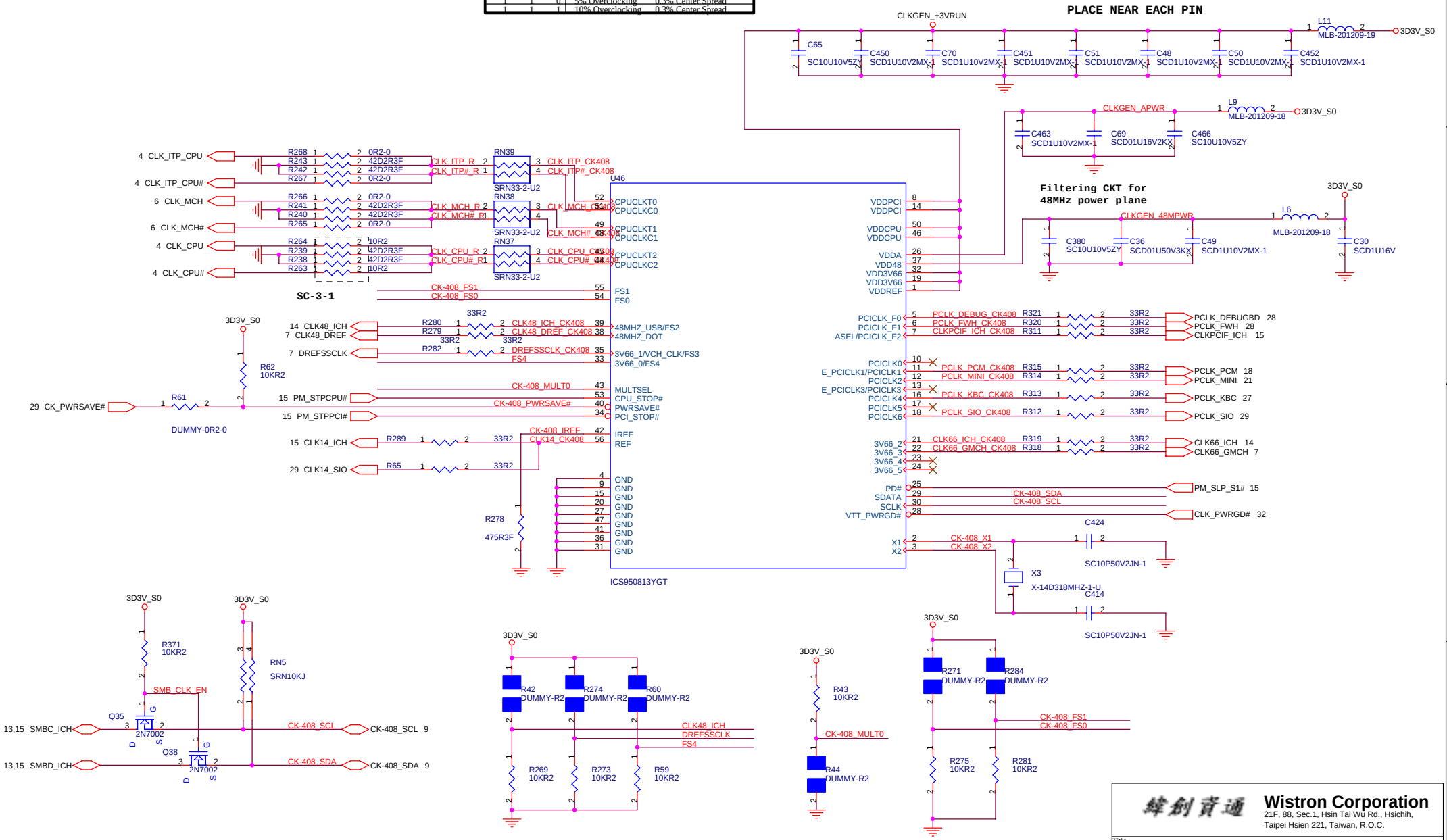
Size: A3 | Document Number: A1+ | Rev: SA

Date: Thursday, December 26, 2002 | Sheet 2 of 39

Freq. Setting

FS1	FS0	CPU	AGP	PCI
0	0	100.00	66.66	33.33
0	1	133.33	66.66	33.33
1	0	200.00	66.66	33.33
1	1	166.66	66.66	33.33

Freqency Select			CPU,3V66,PCI	
FS4	FS3	FS2		
0	0	0	Standard Clocking	0.3% Center Spread
0	0	1	Standard Clocking	0 to -0.5%, Down Spread
0	1	0	Standard Clocking	0.3% Center Spread
0	1	1	Standard Clocking	0 to - 0.75%, Down Spread
1	0	0	Pwr Save Clocking	Spread Off
1	0	1	3% Overclocking	0.3% Center Spread
1	1	0	5% Overclocking	0.3% Center Spread
1	1	1	10% Overclocking	0.3% Center Spread



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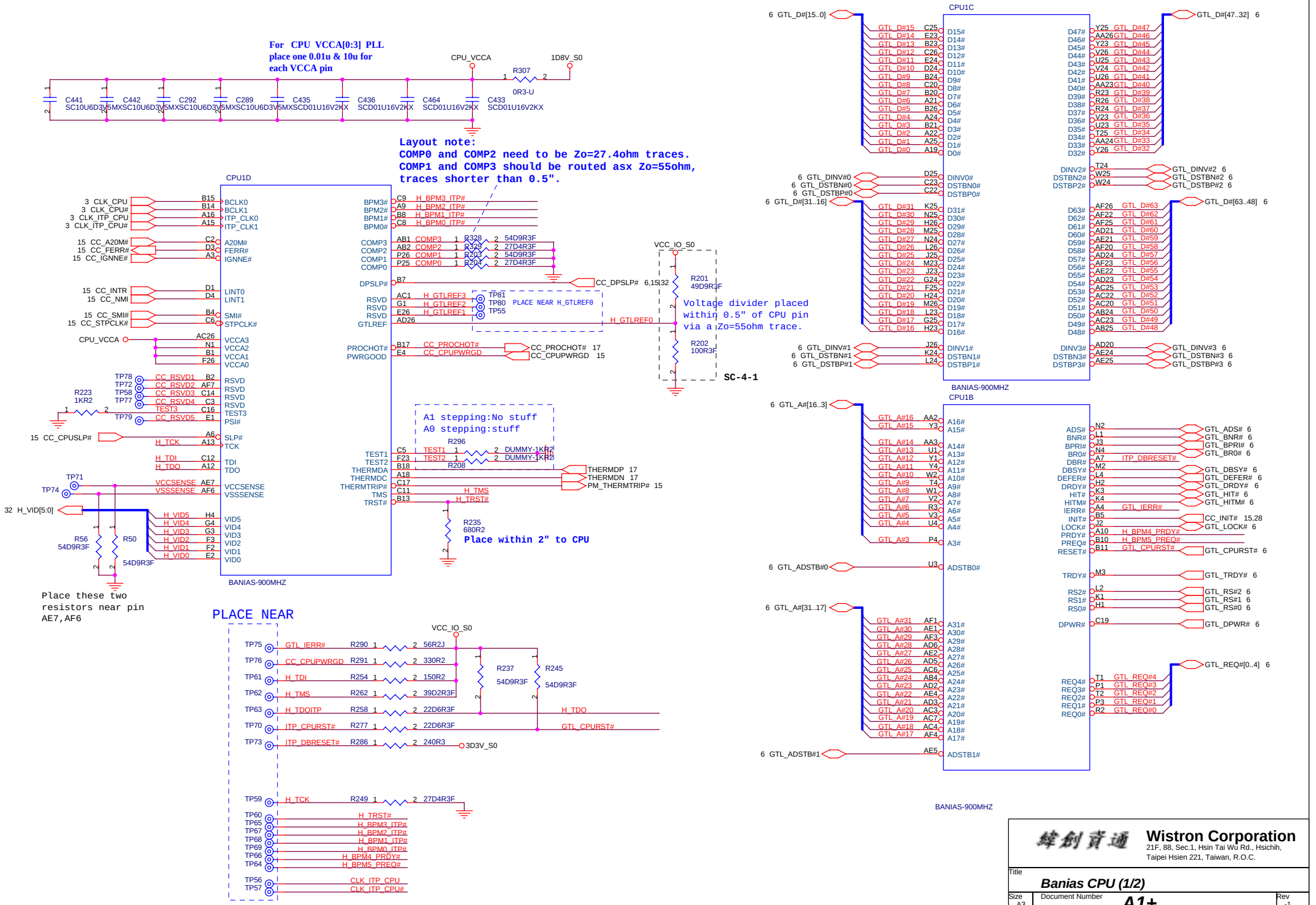
Title: CLOCK GEN.

Size: A3 | Document Number: A1+ | Rev: -1

Date: Thursday, June 19, 2003 | Sheet 3 of 39



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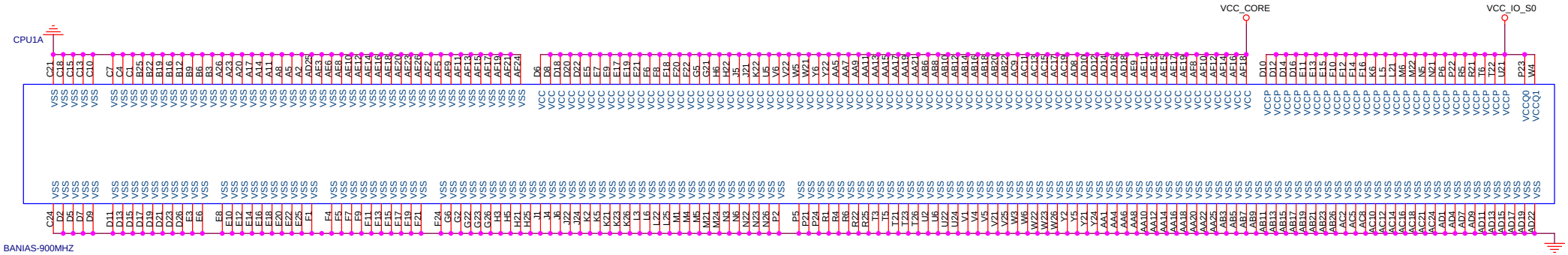
Title: Banias CPU (1/2)

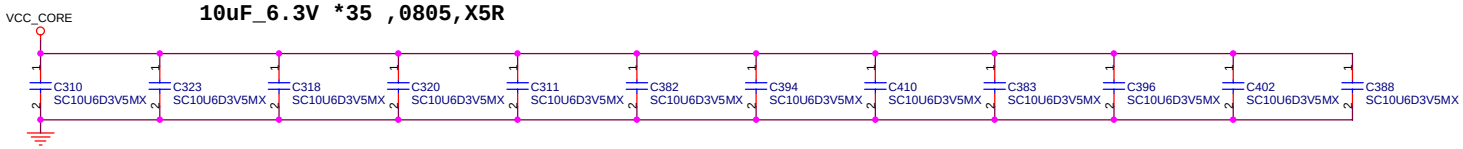
Size: A3 | Document Number: A1+ | Rev: -1

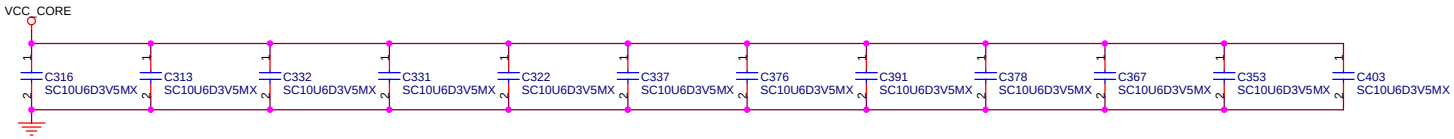
Date: Thursday, June 19, 2003 | Sheet 4 of 39

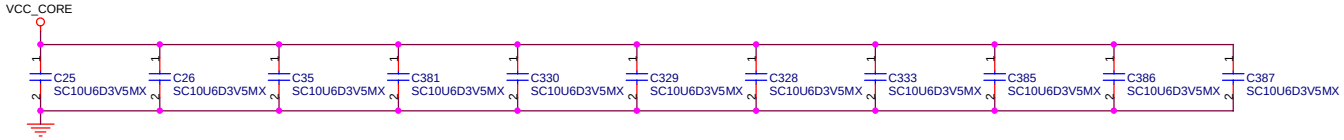
Ref 10598 EMTS
P69 need place
Decoupling
near between
VCCQ ???



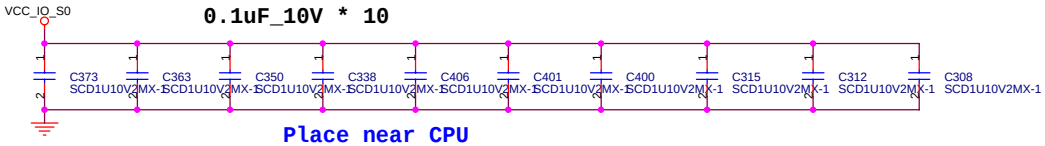
10uF_6.3V *35 ,0805,X5R







0.1uF_10V * 10



Place near CPU

緯創資通 Wistron Corporation
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Title	*Banias CPU (2/2)*		
Size A3	Document Number *A1+*		Rev -1
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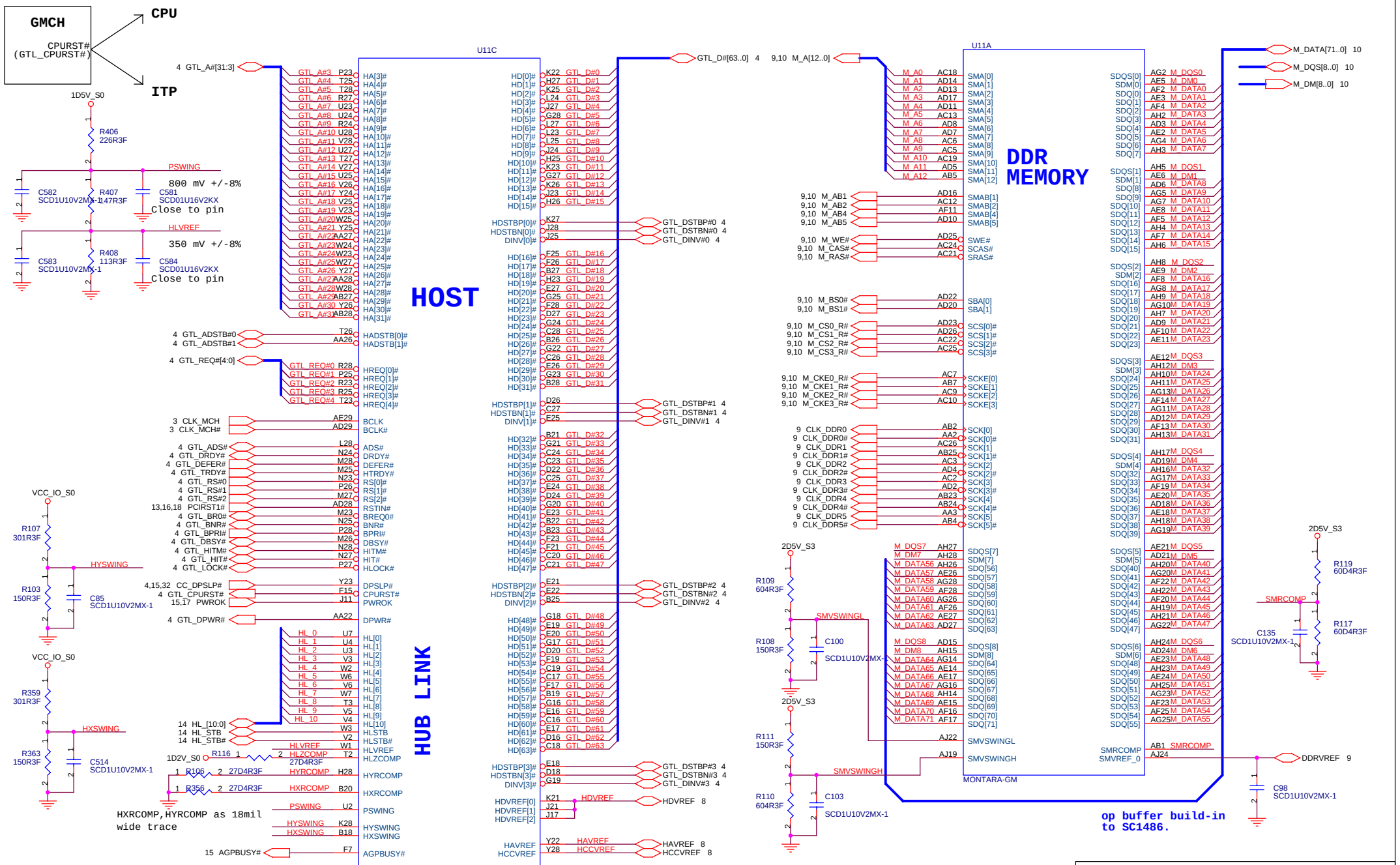

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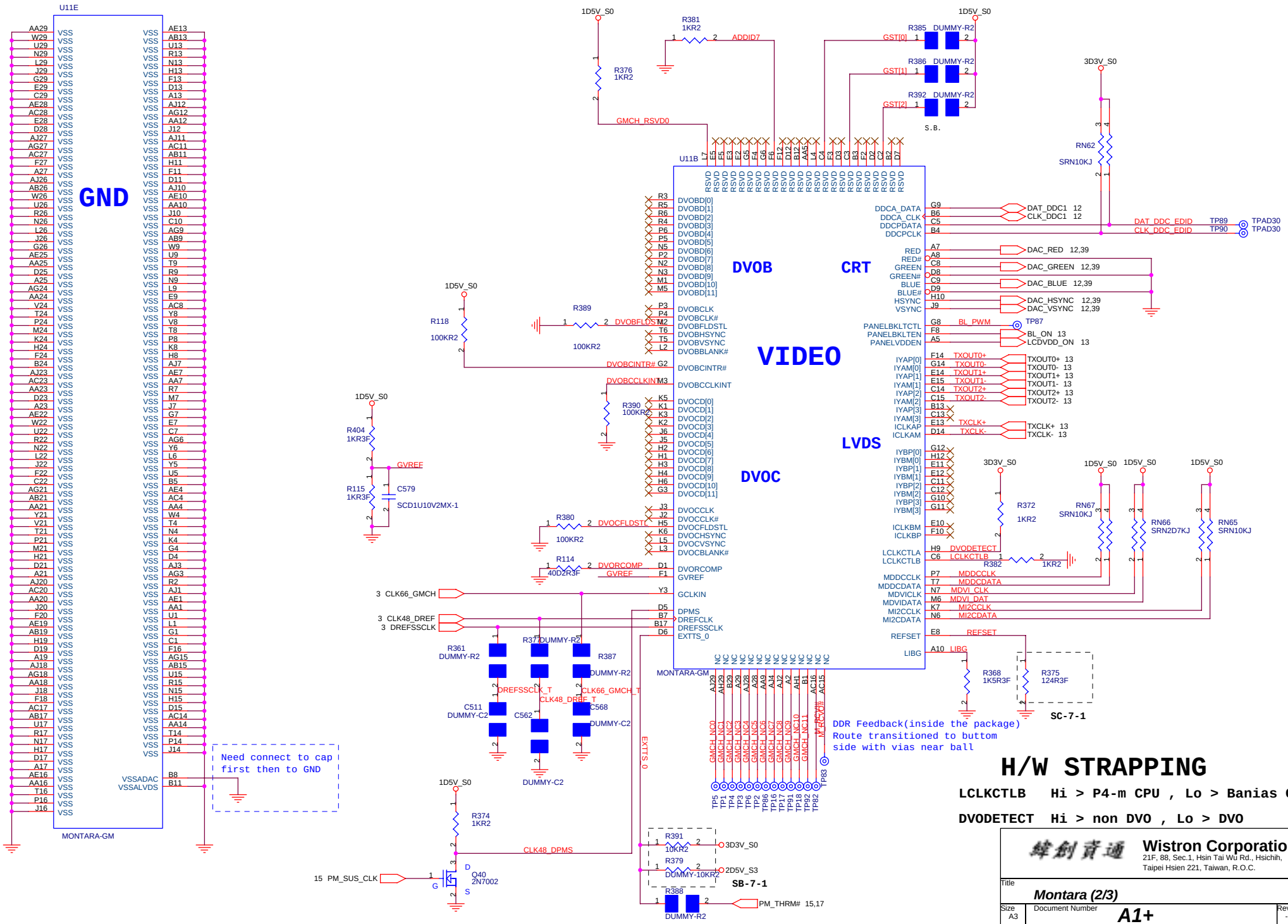
Taipei Hsien 221, Taiwan, R.O.C.

Title: Montara (1/3)

Size: A3 | Document Number: A1+ | Rev: -1

Date: Wednesday, July 09, 2003 | Sheet 6 of 39



H/W STRAPPING

LCLKCTLB Hi > P4-m CPU , Lo > Banias CPU

DVODETECT Hi > non DVO , Lo > DVO

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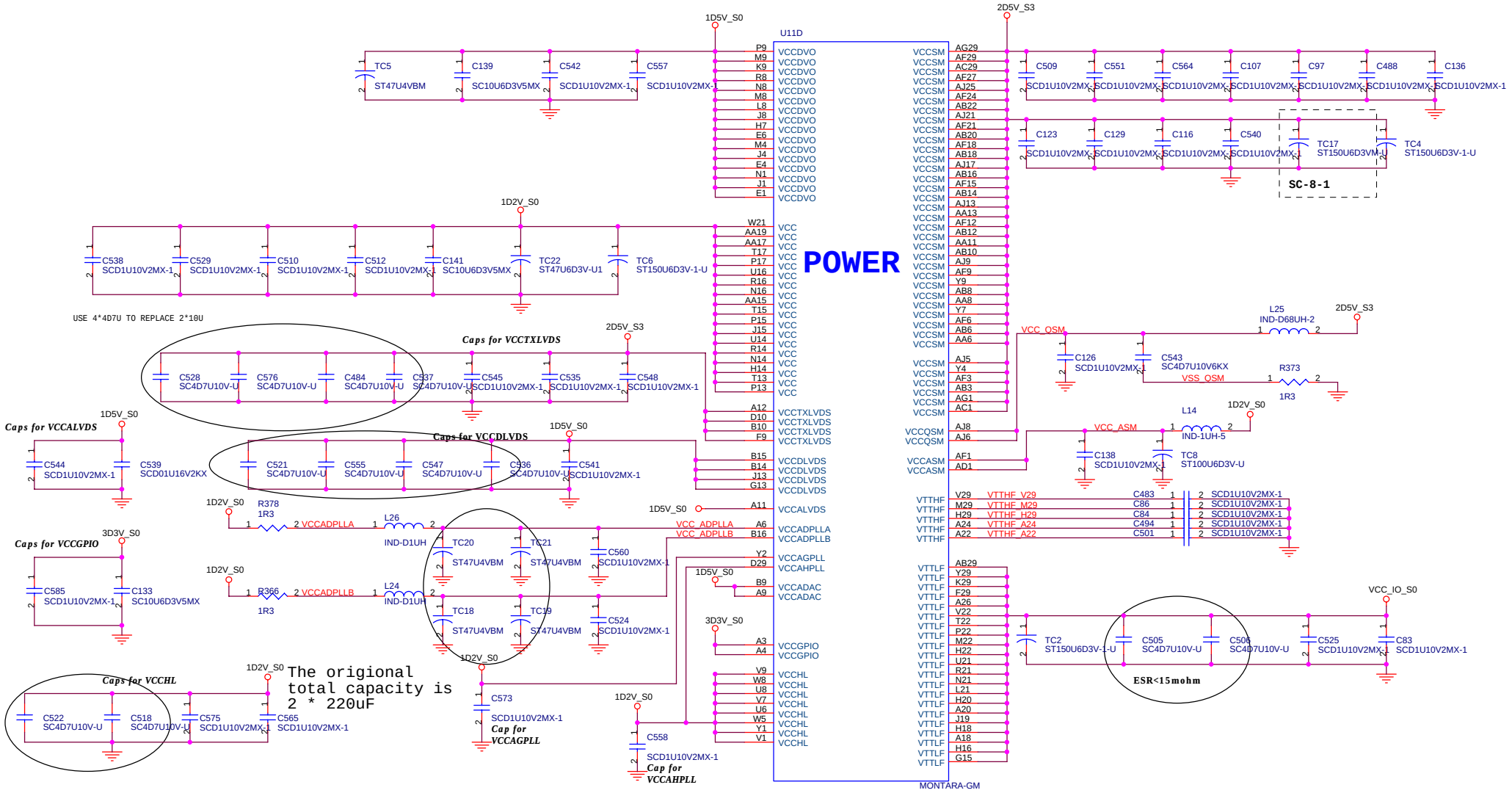
Title: *Montara (2/3)*

Size: A3 | Document Number: *A1+* | Rev: -1

Date: Wednesday, July 09, 2003 | Sheet 7 of 39



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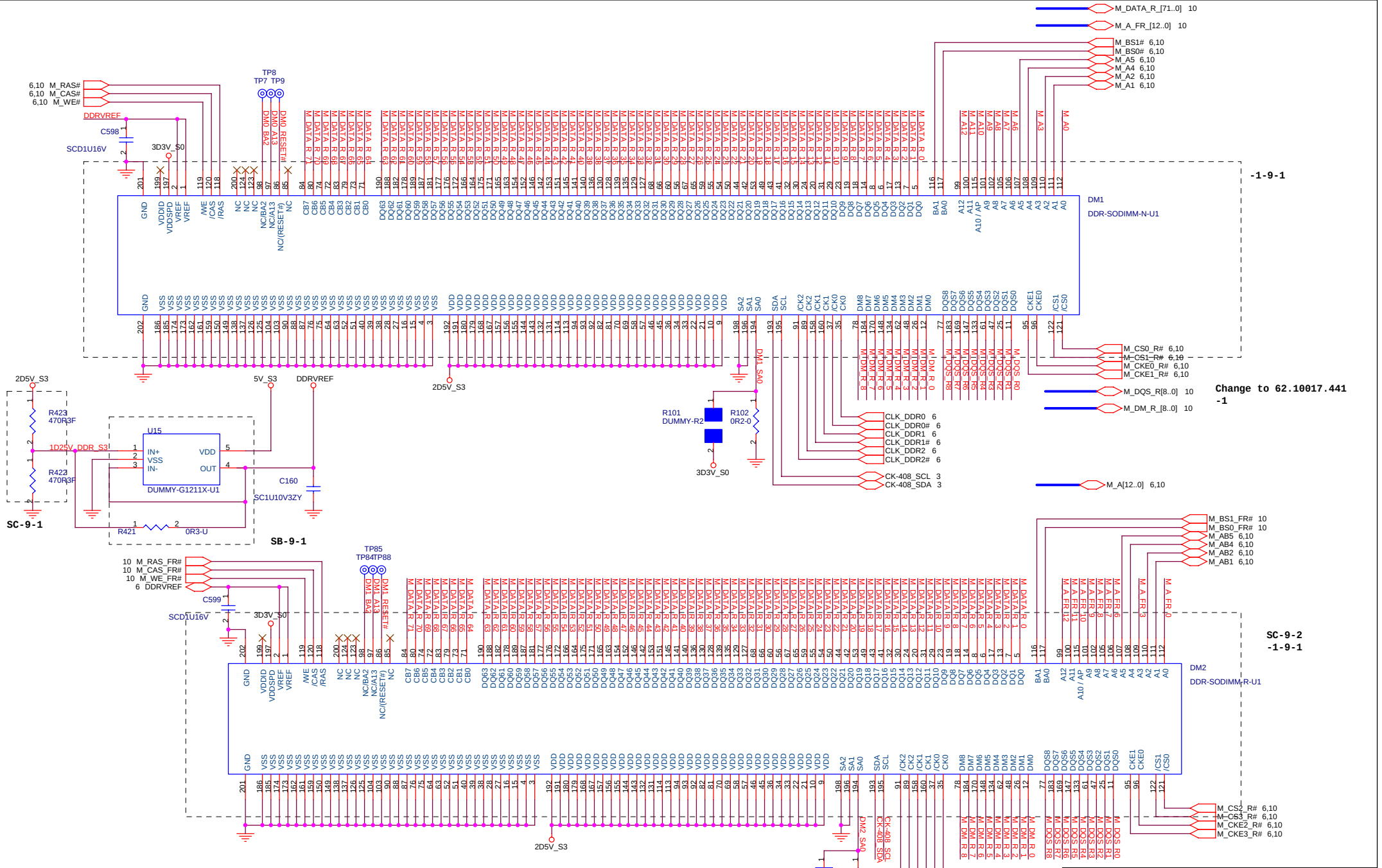
Title: Montara (3/3)

Size: A3 | Document Number: A1+ | Rev: -1

Date: Wednesday, July 09, 2003 | Sheet 8 of 39



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Title: **DDR Socket**

Size: A3 | Document Number: **A1+** | Rev: -1

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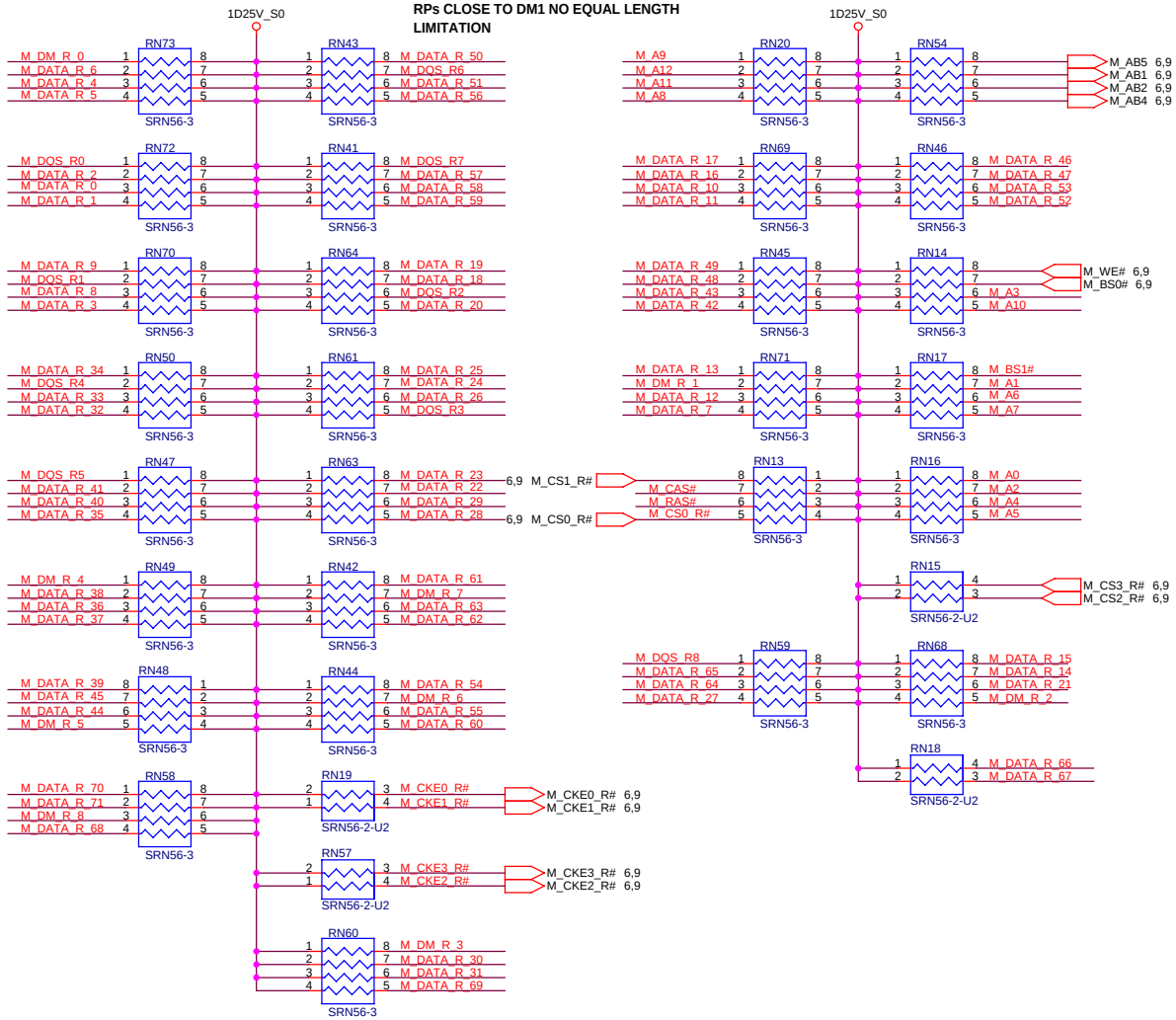
SERIES DAMPING

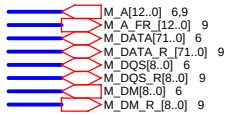
PLACE RNs CLOSE TO DM0, < 0.75"
STRICT EQUAL LENGTH
LIMITATION WITH DQS, CB PINS

PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", Command <0.25",PLACE
RPs CLOSE TO DM1 NO EQUAL LENGTH
LIMITATION



Control signals use Topology 2



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Title: DDR Serial/Terminator Resistor

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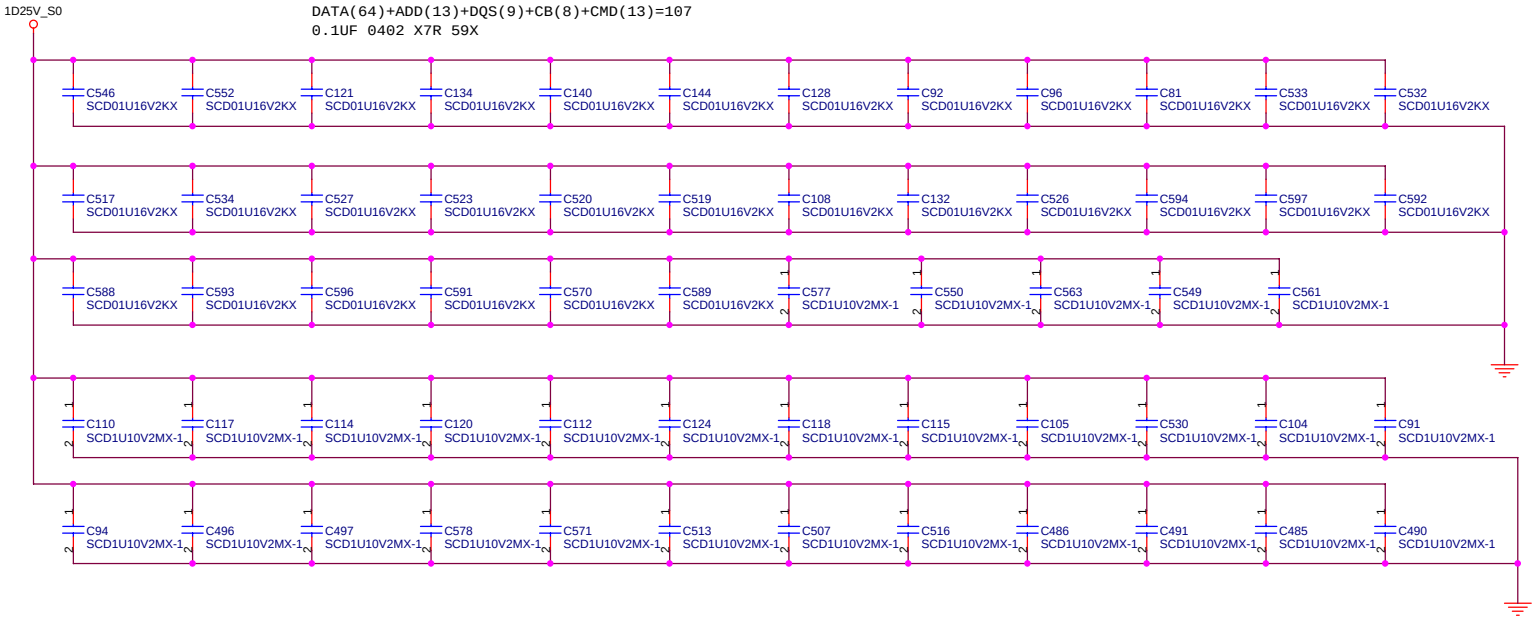
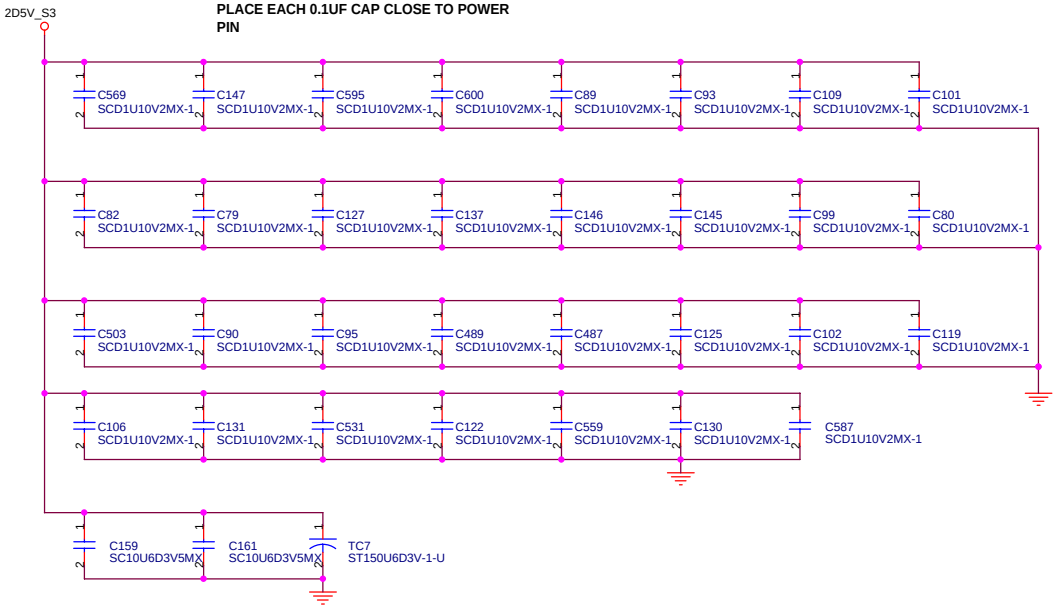
PLACE ONE 0.1 and ONE 0.01 CAP CLOSE TO EVERY 4
PULL-UP TERMINATION RESISTORS, CRB-P13
DATA(64)+ADD(13)+DQS(9)+CB(8)+CMD(13)=107
0.1UF 0402 X7R 59X



PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER
PIN



緯創資通 **Wistron Corporation**
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Title	***DDR Decoupling CAP***	
Size A3	Document Number ***A1+***	Rev -1
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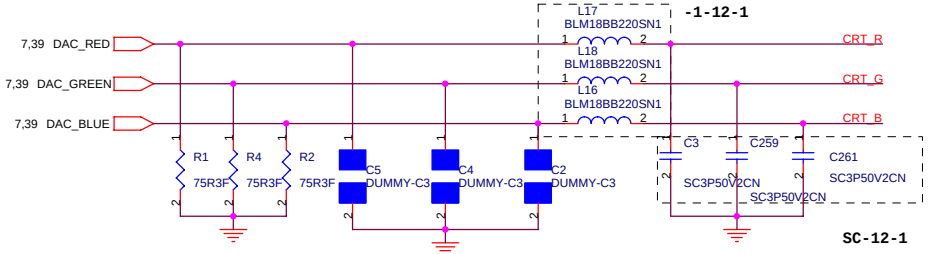
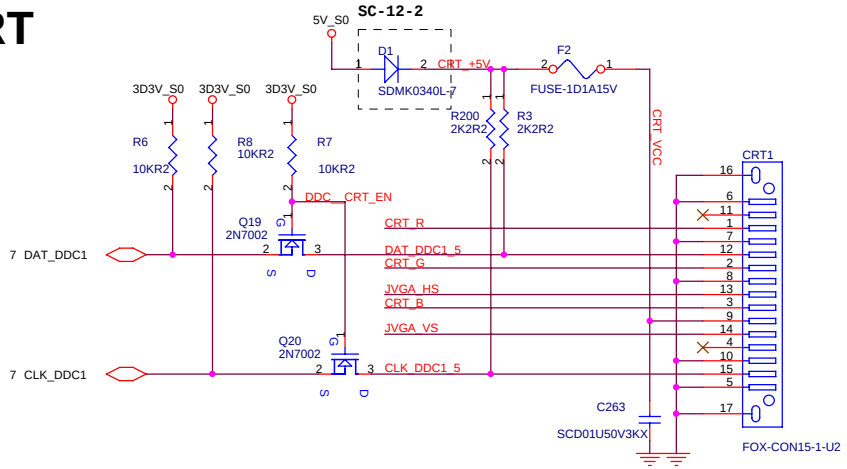
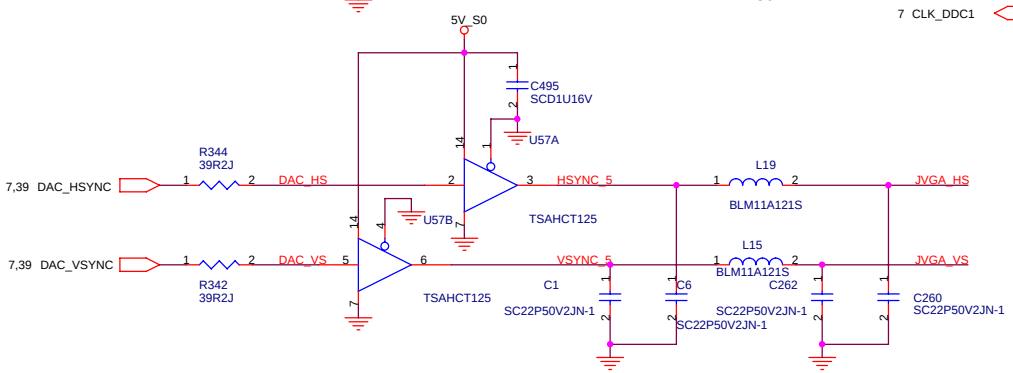
Layout Note:
Must be a ground return path between this ground and the ground on the VGA connector.

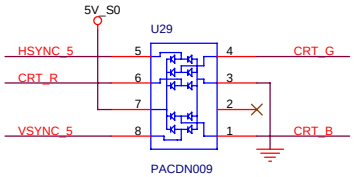
37.4_1% resistors must be placed after RGB pi filter ,near CRT connector.

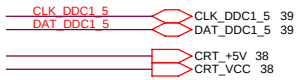
CRT











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Title: CRT CONN.

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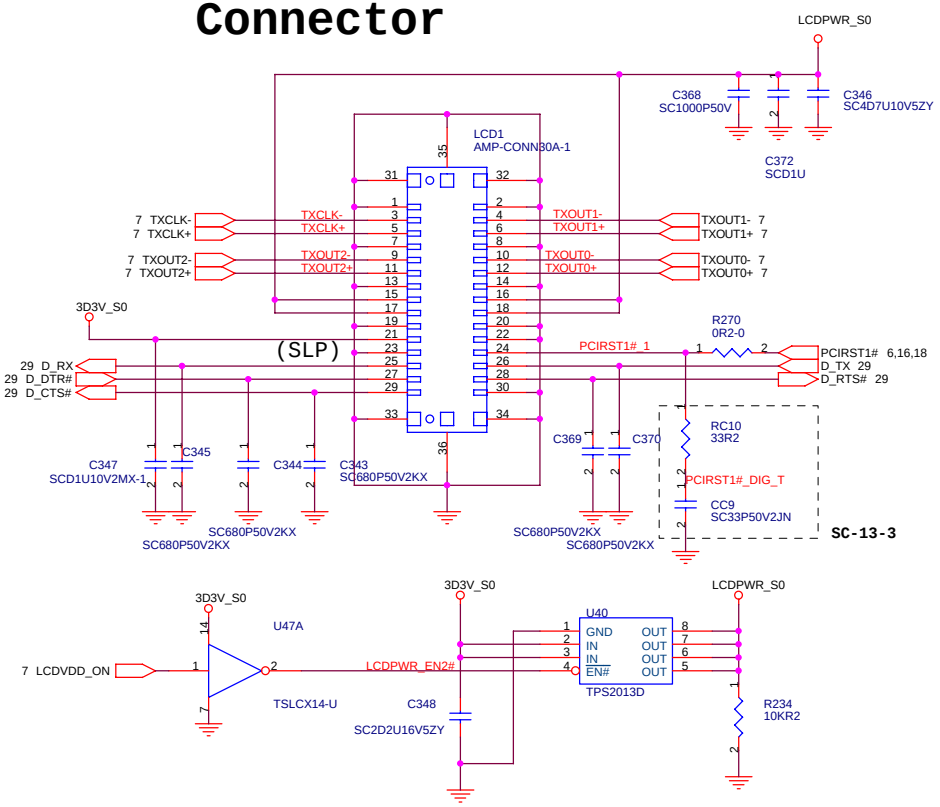
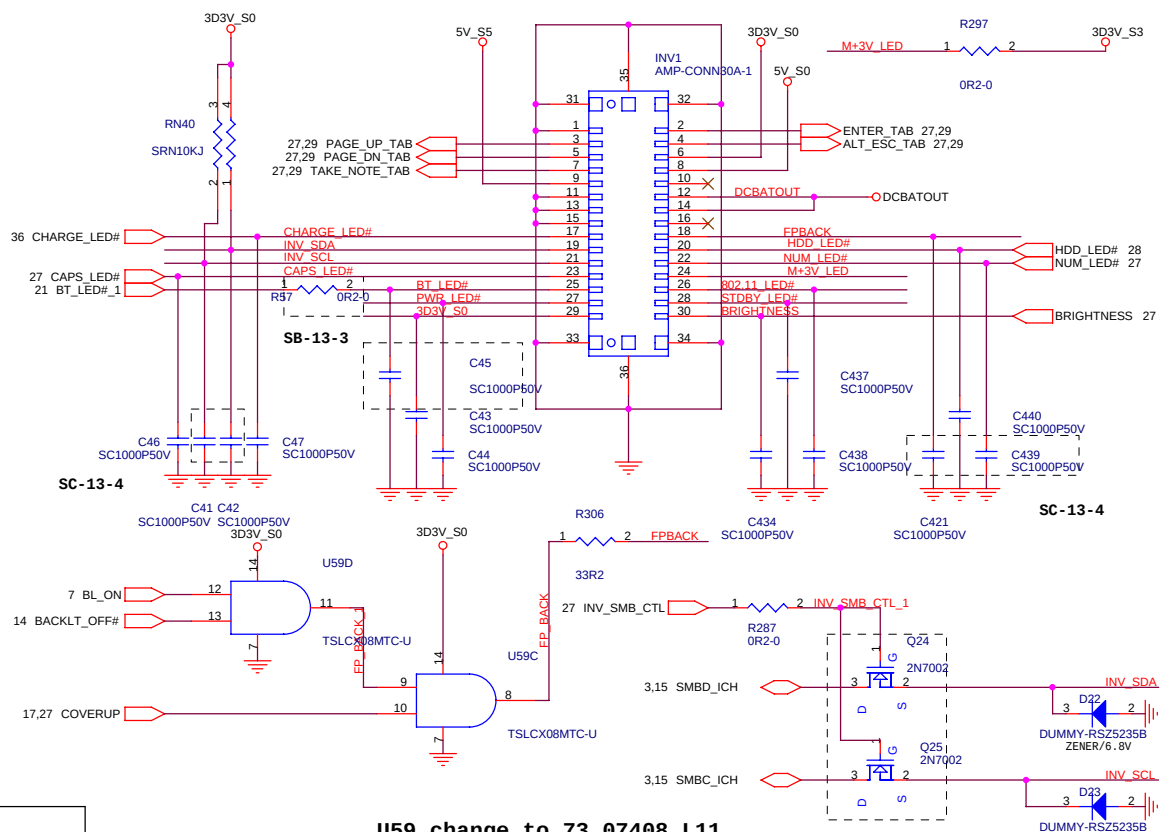
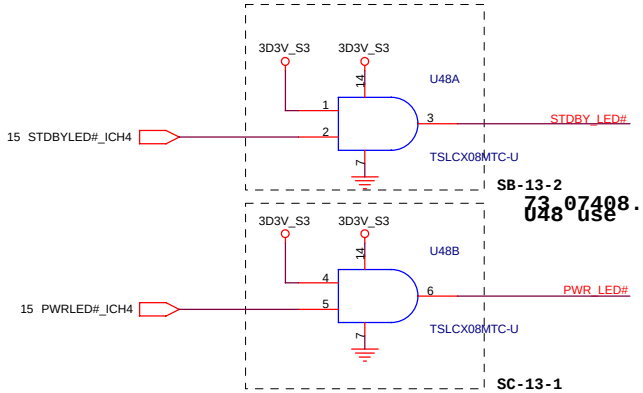
LVDS & DIGITIZER Connector



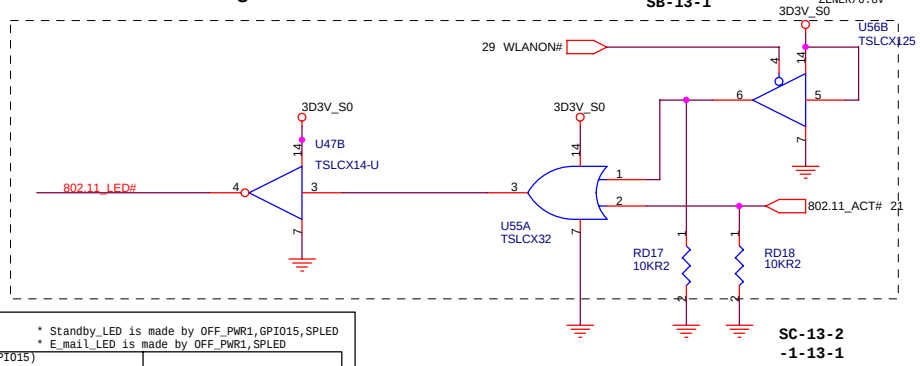
INVERTER & LED & BUTTOM Connector



U59 change to 73.07408.L11



73.07408.L11 U48 use



* Standby_LED is made by OFF_PWR1,GPIO15,SPLED
* E_mail_LED is made by OFF_PWR1,SPLED

	(GPO36) E_MAIL	(GPIO7) STDBY	(GPIO15) ENSTDBY#_5	SPLED	Standby_LED	E_mail_LED
POWER_ON DFAULT	H	H	H	L	OFF	OFF
S0 without E_mail LED	L	H	H	Flash	OFF	OFF
S0 with E_mail LED	H	H	H	Flash	OFF	Flash
S1 without E_mail LED	L	L	L	Flash	ON	OFF
S1 with E_mail LED	L/H	L	L	Flash	ON	OFF/Flash
Enter/Leave S3 without E_mail LED	L	H	L	Flash	Flash	OFF (Decide by BIOS)
Enter/Leave S3 with E_mail LED	L	H	L	Flash	Flash	OFF
S3	L	L	L	L	ON	OFF
Enter/Leave S4 without E_mail LED	L	H	L	Flash	Flash	
Enter/Leave S4 with E_mail LED	L	H	L	Flash	Flash	OFF
S4	L	L	NO POWER	L	OFF	OFF

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Title: **LCD Power/Inverter**

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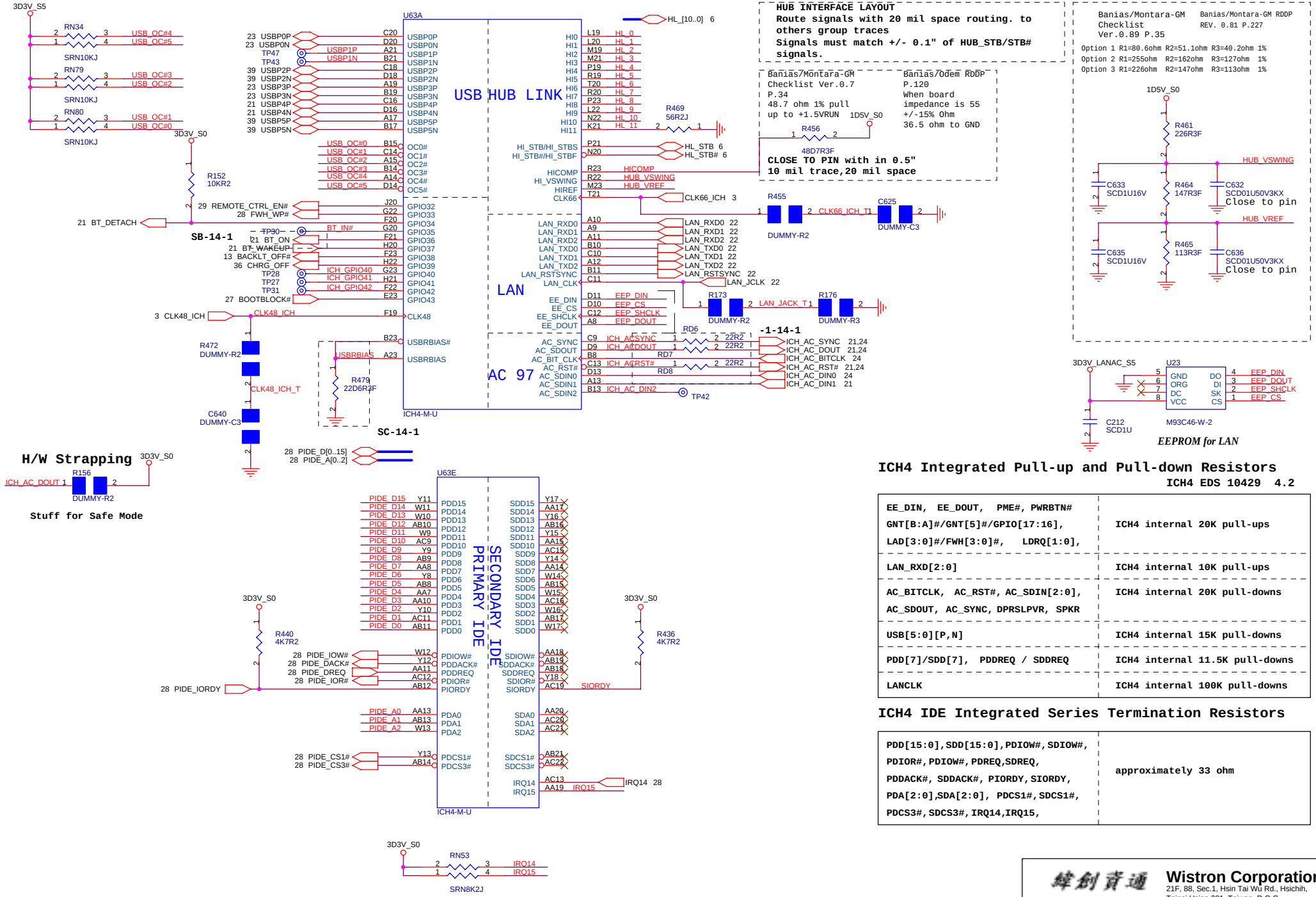

ICH4 Integrated Pull-up and Pull-down Resistors

ICH4 EDS 10429 4.2

EE_DIN, EE_DOUT, PME#, PWRBTN# GNT[B:A]#/GNT[5]#/GPIO[17:16], LAD[3:0]#/FWH[3:0]#, LDRQ[1:0],	ICH4 internal 20K pull-ups
LAN_RXD[2:0]	ICH4 internal 10K pull-ups
AC_BITCLK, AC_RST#, AC_SDIN[2:0], AC_SDOUT, AC_SYNC, DPRSLPVR, SPKR	ICH4 internal 20K pull-downs
USB[5:0][P,N]	ICH4 internal 15K pull-downs
PDD[7]/SDD[7], PDDREQ / SDDREQ	ICH4 internal 11.5K pull-downs
LANCLK	ICH4 internal 100K pull-downs

ICH4 IDE Integrated Series Termination Resistors

PDD[15:0],SDD[15:0],PDIOW#,SDIOW#, PDIOR#,PDIOW#,PDREQ,SDREQ, PDDACK#, SDDACK#, PIORDY,SIORDY, PDA[2:0],SDA[2:0], PDCS1#,SDCS1#, PDCS3#,SDCS3#,IRQ14,IRQ15,	approximately 33 ohm

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Title: ICH4-M (1/3)

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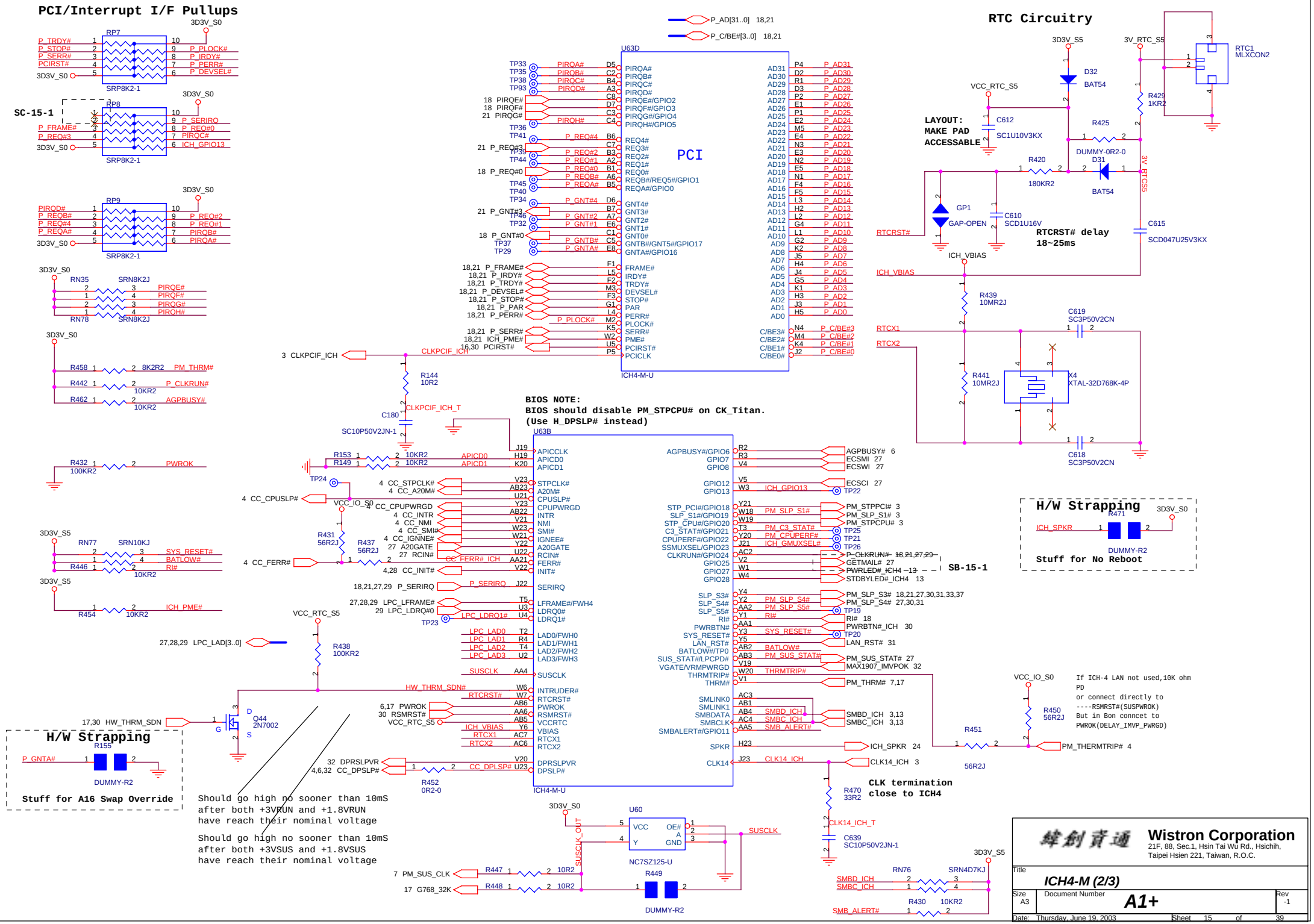
PCI/Interrupt I/F Pullups
RP7
SRP8K2-1
SC-15-1
RP8
RP9
RN35
SRN8K2J
RN78
R458 8K2R2 PM_THRM#
R442 10KR2 P_CLKRUN#
R462 10KR2 AGPBUSY#
R432 100KR2 PWROK
RN77
SRN10KJ
R446 10KR2 RI#
R454 10KR2 ICH_PME#
U63D
PCI
ICH4-M-U
P_AD[31..0] 18,21
P_C/BE#[3..0] 18,21
RTC Circuitry
RTC1 MLXCON2
D32 BAT54
R429 1KR2
R425 DUMMY-0R2-0
D31 BAT54
R420 180KR2
C612 SC1U10V3KX
C610 SCD1U16V
C615 SCD047U25V3KX
GP1 GAP-OPEN
LAYOUT: MAKE PAD ACCESSABLE
RTCRST# delay 18~25ms
R439 10MR2J
C619 SC3P50V2CN
R441 10MR2J
X4 XTAL-32D768K-4P
C618 SC3P50V2CN
R144 10R2
C180 SC10P50V2JN-1
BIOS NOTE:
BIOS should disable PM_STPCPU# on CK_Titan.
(Use H_DPSLP# instead)
U63B
R153 10KR2
R149 10KR2
R431 56R2J
R437 56R2J
R438 100KR2
Q44 2N7002
H/W Strapping
R155 DUMMY-R2
Stuff for A16 Swap Override
Should go high no sooner than 10mS after both +3VRUN and +1.8VRUN have reach their nominal voltage
Should go high no sooner than 10mS after both +3VSUS and +1.8VSUS have reach their nominal voltage
R452 0R2-0
U60
NC7SZ125-U
R449 DUMMY-R2
R447 10R2
R448 10R2
SB-15-1
H/W Strapping
R471 DUMMY-R2
Stuff for No Reboot
R450 56R2J
R451 56R2J
If ICH-4 LAN not used,10K ohm PD
or connect directly to
----RSMRST#(SUSPWROK)
But in Bon conncet to
PWROK(DELAY_IMVP_PWRGD)
R470 33R2
CLK termination close to ICH4
C639 SC10P50V2JN-1
RN76
SRN4D7KJ
R430 10KR2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH4-M (2/3)
Size A3
Document Number A1+
Rev -1
Date: Thursday, June 19, 2003
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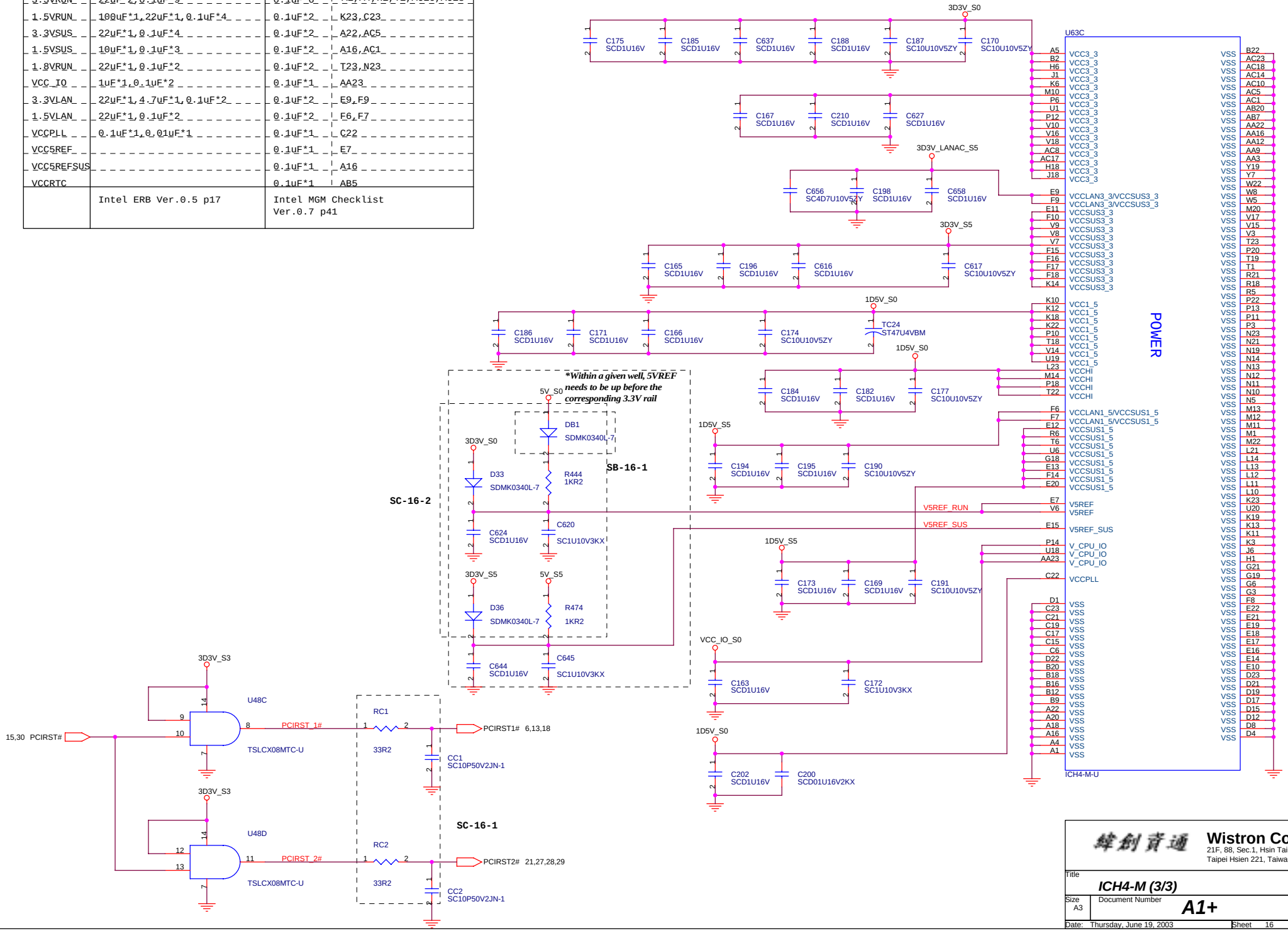
		Near Balls	
3.3VRUN	22uF*2,0.1uF*9	0.1uF*6	A1,A4,H1,T1,AC10,AC18
1.5VRUN	100uF*1,22uF*1,0.1uF*4	0.1uF*2	K23,C23
3.3VSUS	22uF*1,0.1uF*4	0.1uF*2	A22,AC5
1.5VSUS	10uF*1,0.1uF*3	0.1uF*2	A16,AC1
1.8VRUN	22uF*1,0.1uF*2	0.1uF*2	T23,N23
VCC_IO	1uF*1,0.1uF*2	0.1uF*1	AA23
3.3VLAN	22uF*1,4.7uF*1,0.1uF*2	0.1uF*2	E9,F9
1.5VLAN	22uF*1,0.1uF*2	0.1uF*2	F6,F7
VCCPLL	0.1uF*1,0.01uF*1	0.1uF*1	C22
VCC5REF		0.1uF*1	E7
VCC5REFSUS		0.1uF*1	A16
VCCRTC		0.1uF*1	AB5
	Intel ERB Ver.0.5 p17	Intel MGM Checklist Ver.0.7 p41	

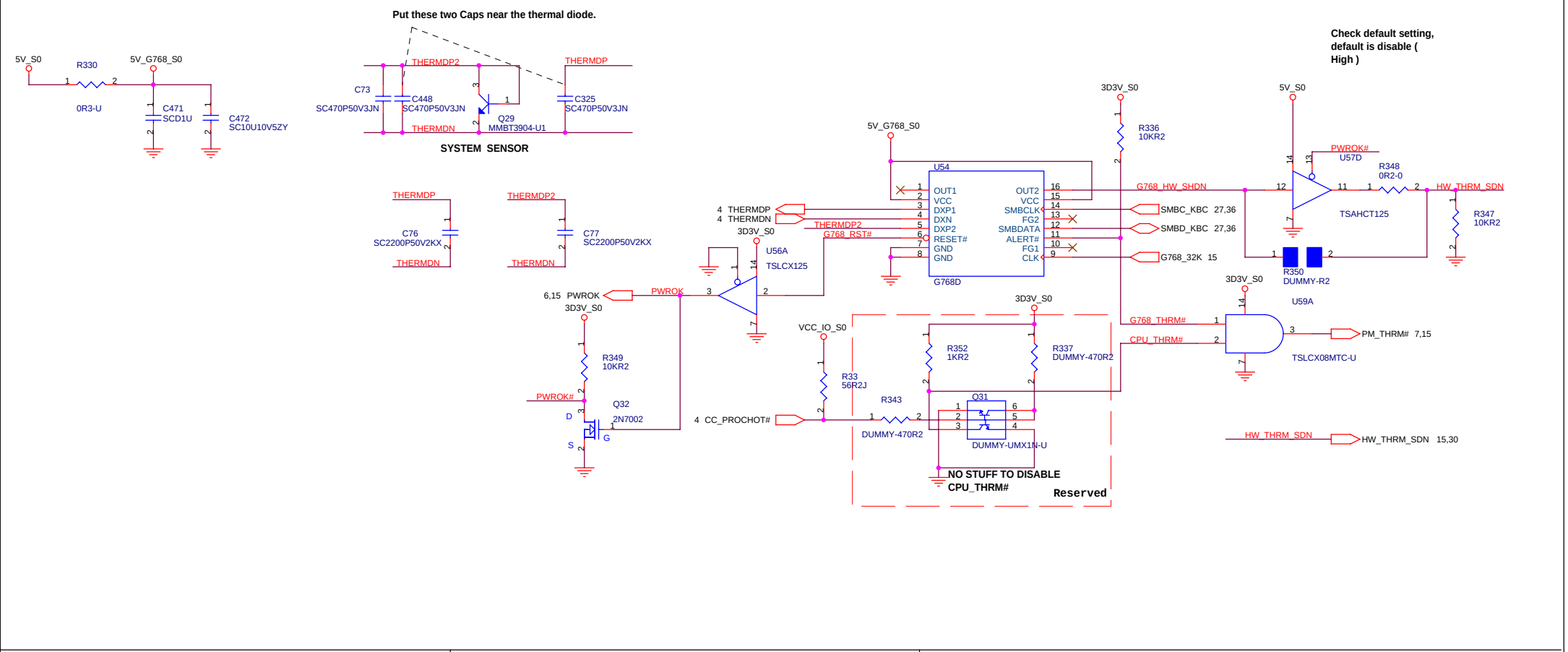


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

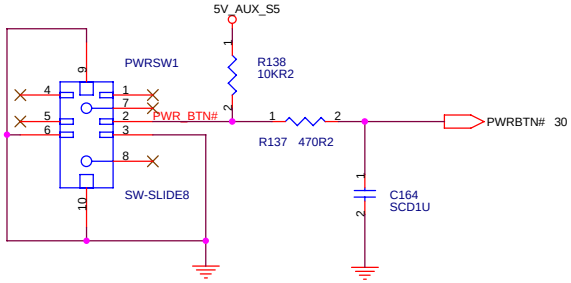
Title: ICH4-M (3/3)

Size: A3 | Document Number: A1+ | Rev: -1

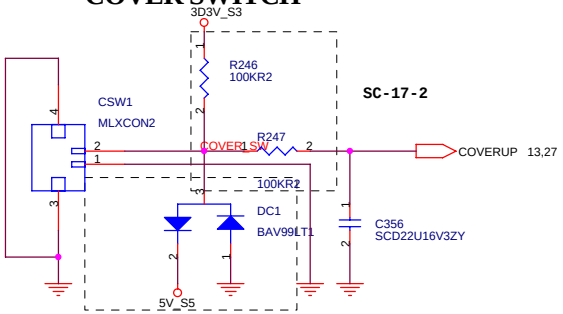
Date: Thursday, June 19, 2003 | Sheet 16 of 39



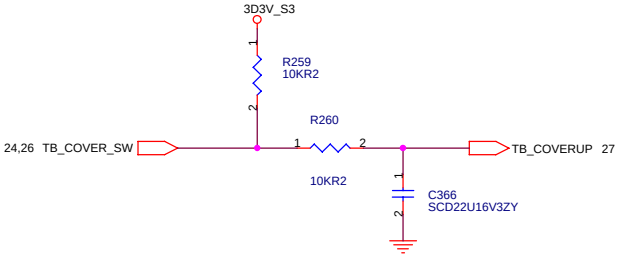
POWER SWITCH



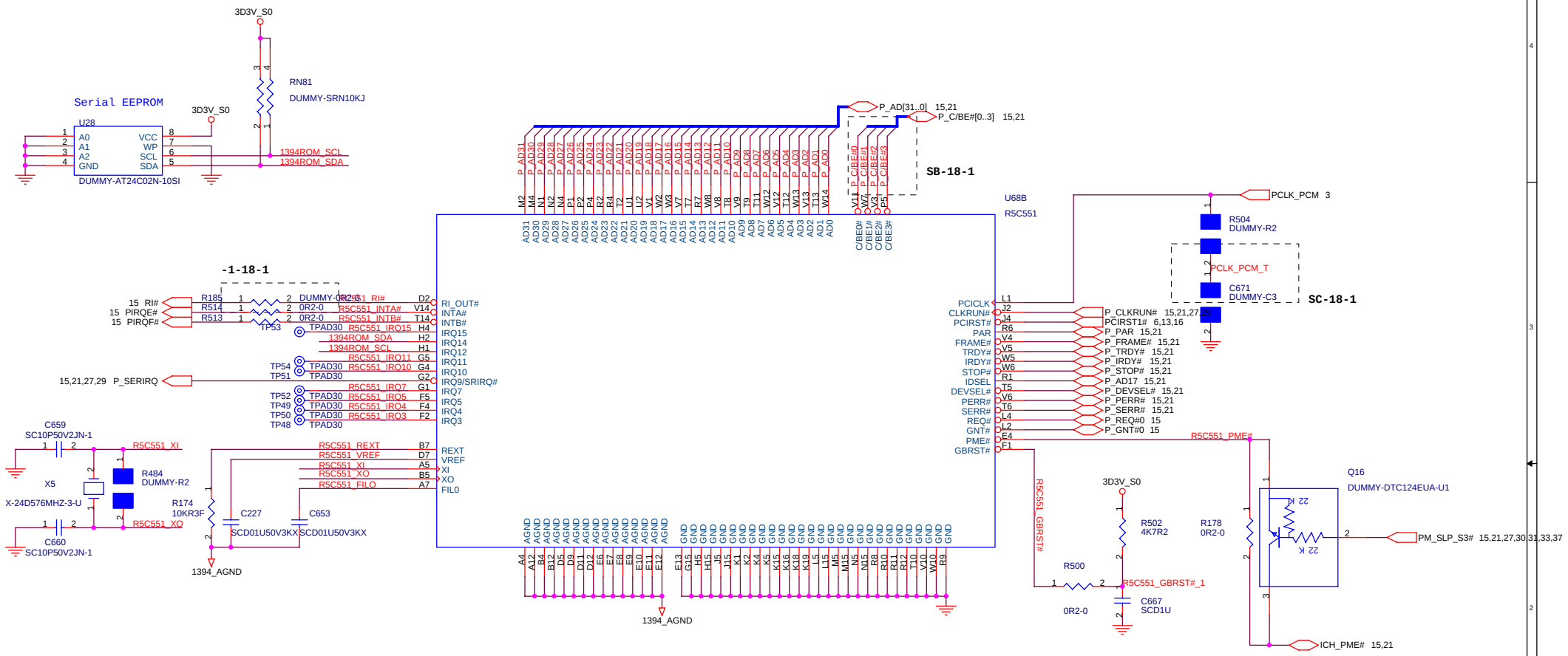
COVER SWITCH



TABLET COVER SWITCH



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***G768D***		
Size A3	Document Number ***A1+***		Rev SC
Date: Thursday, June 19, 2003	Sheet 17 of 39		

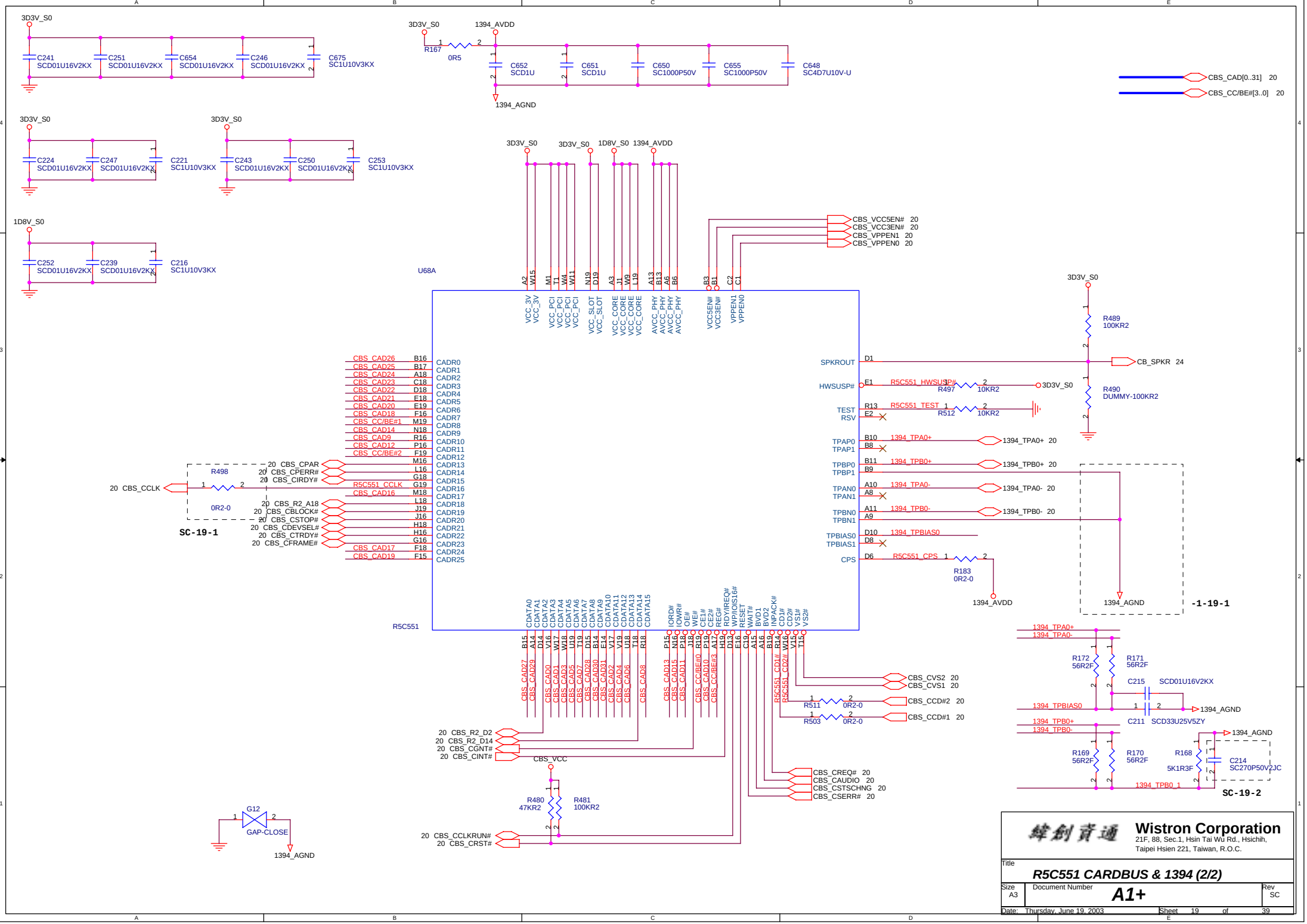


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***R5C551 CARDBUS & 1394 (1/2)***

Size: A3 | Document Number: ***A1+*** | Rev: -1

Date: Thursday, June 19, 2003 | Sheet 18 of 39



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***R5C551 CARDBUS & 1394 (2/2)***

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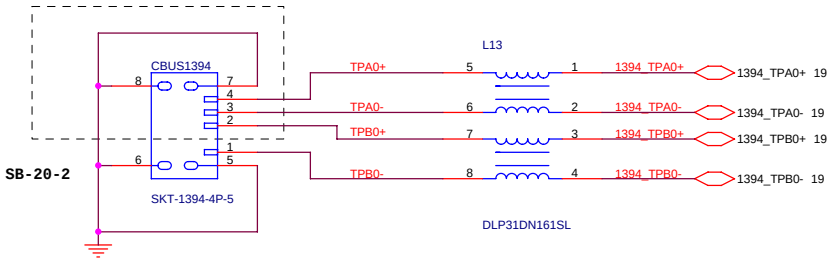
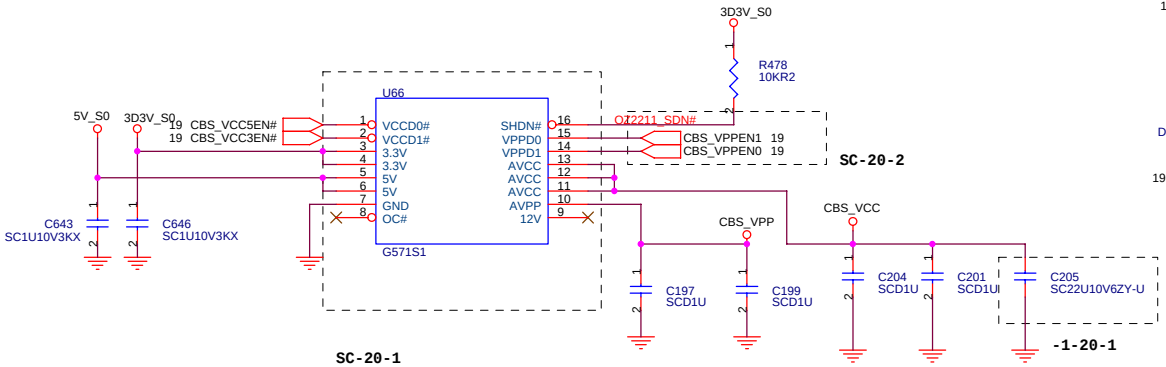
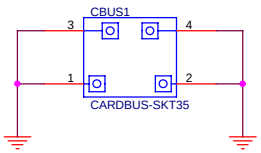
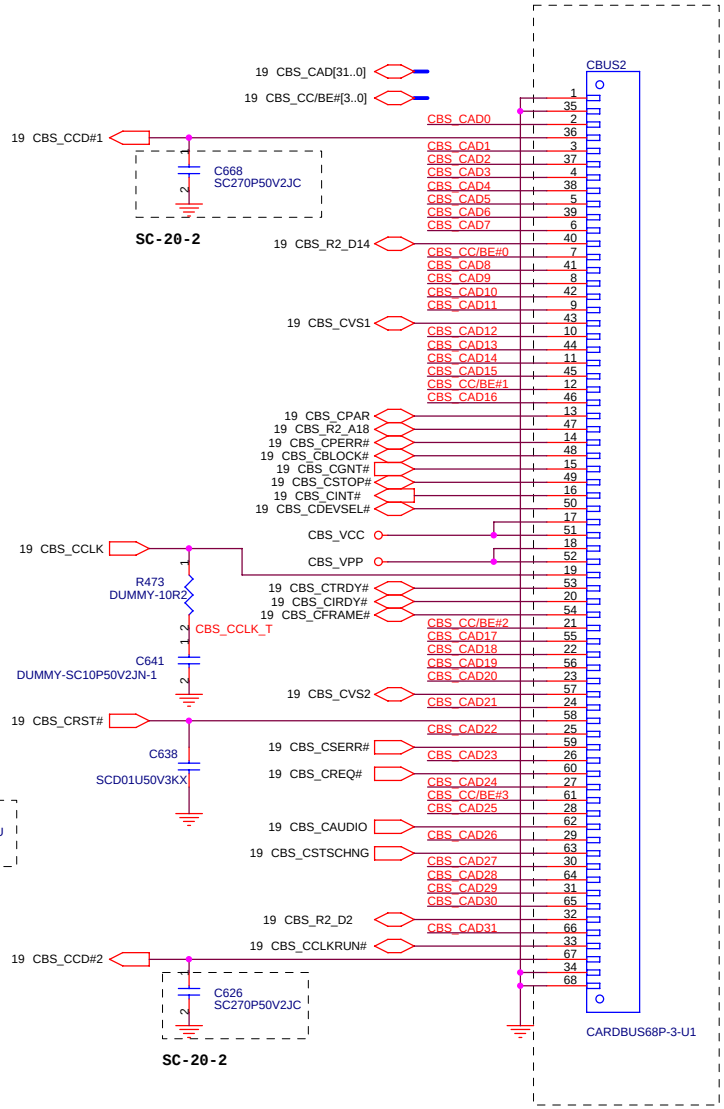
1394 Connector









Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARDBUS CONNECTOR & POWER SWITCH**

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A3	A1+	-1

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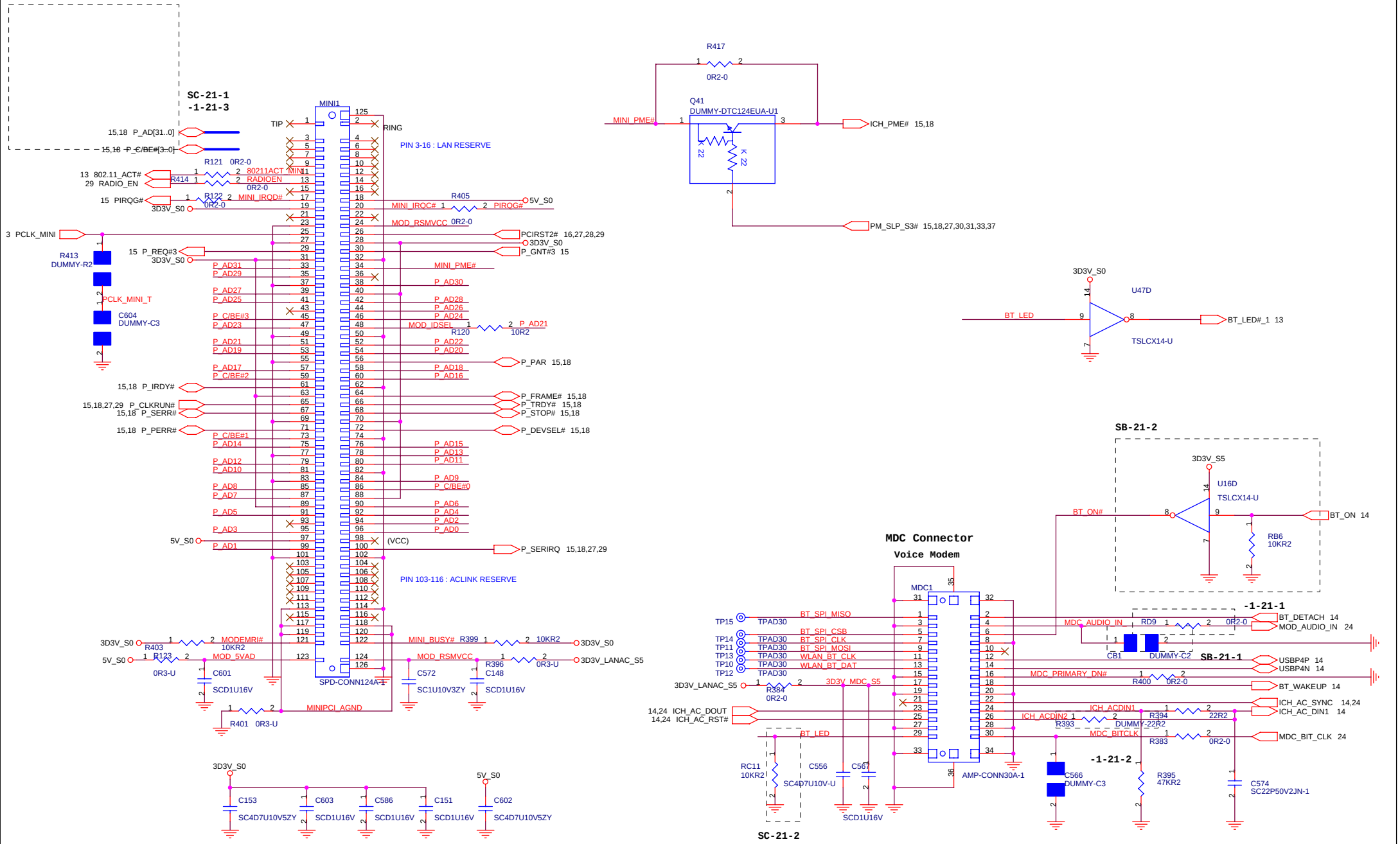

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI PCI (802.11a/b)/MDC/BLUETOOTH***	
Size A3	Document Number ***A1+***	Rev -1
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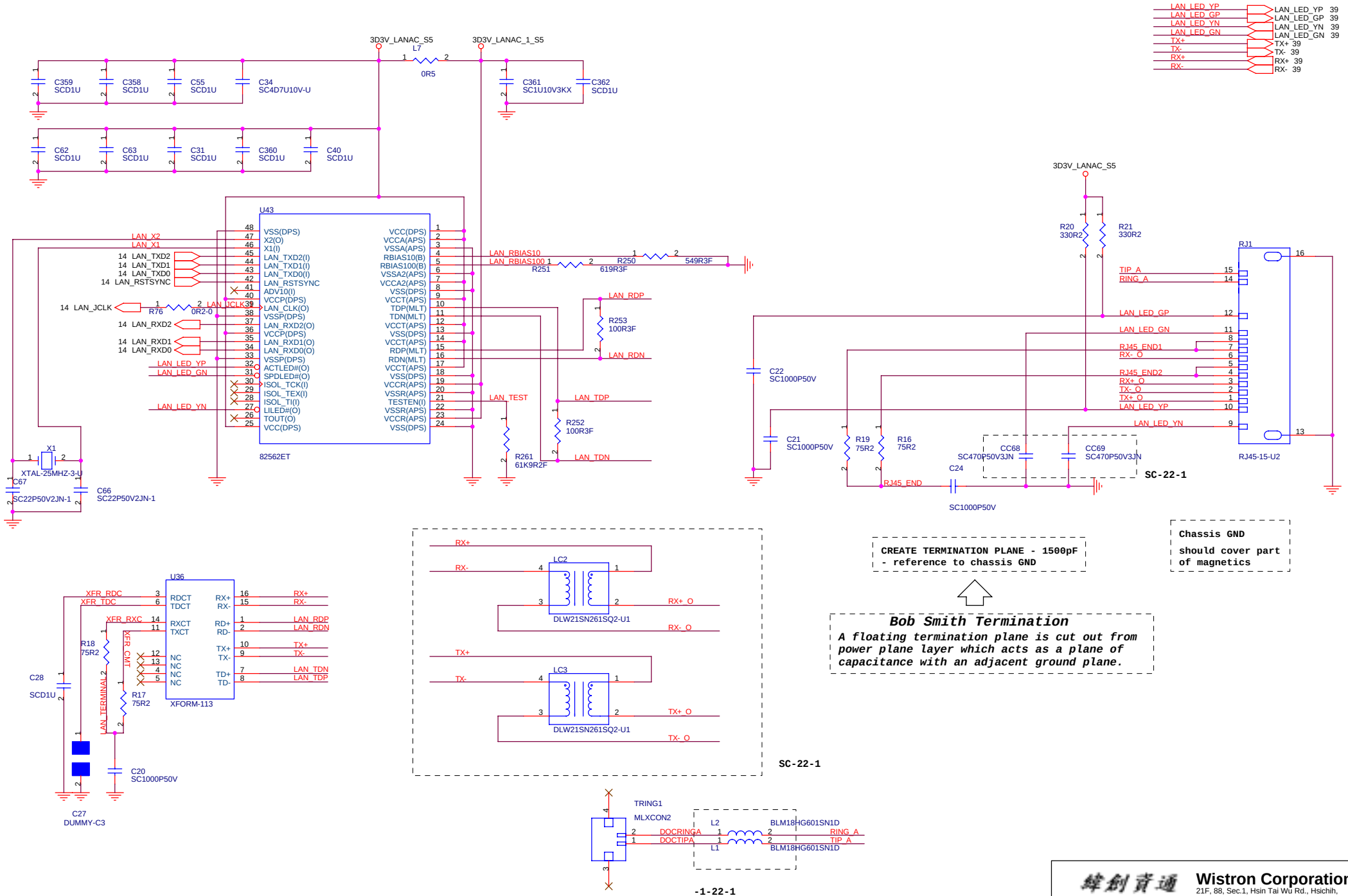

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN PHY

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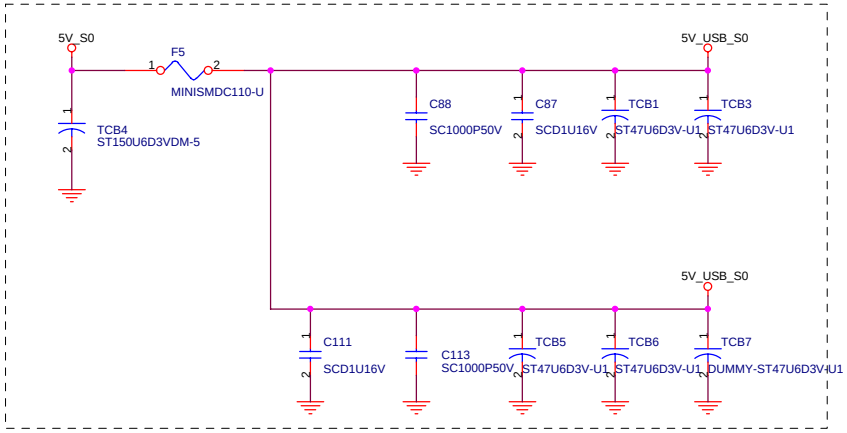
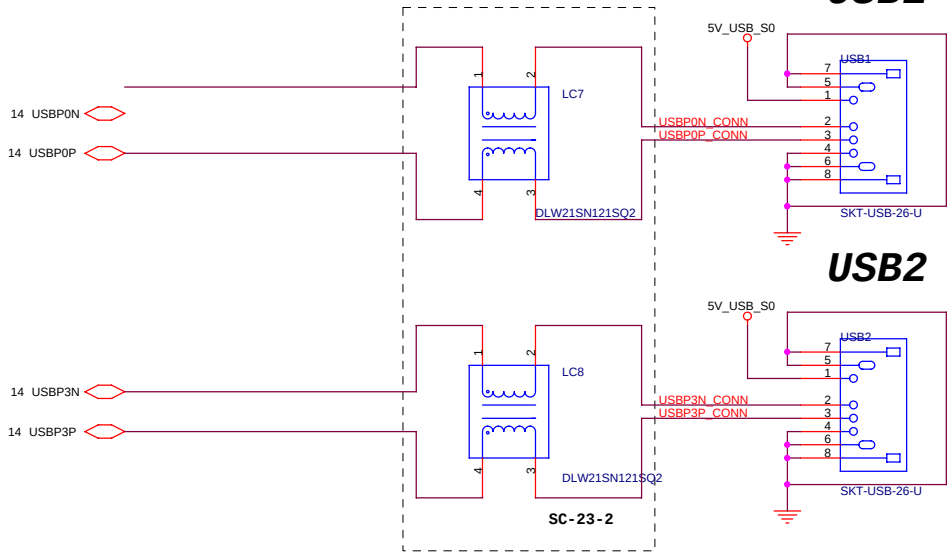
USB 2.0

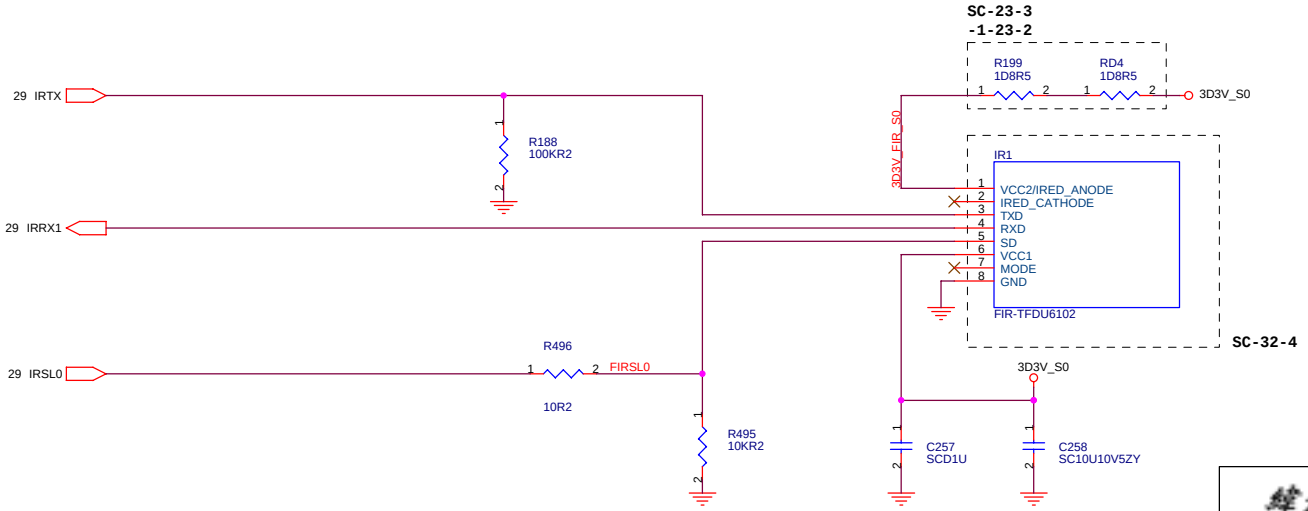


SB-23-1
SC-23-1
-1-23-1

USB1



FIR



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Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 2.0 CONN./FIR

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A3	A1+	-1

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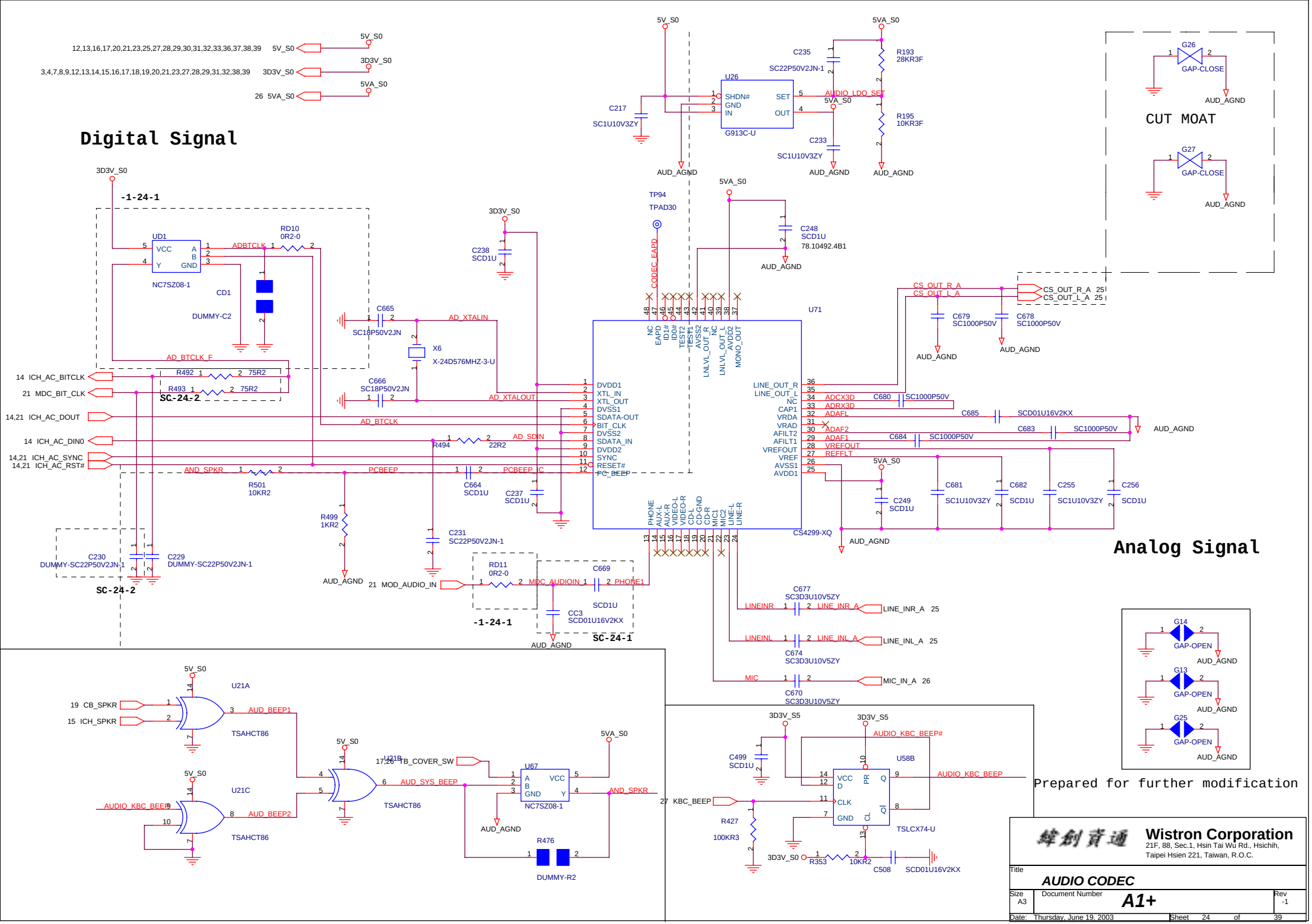
Digital Signal
Analog Signal
CUT MOAT
Prepared for further modification
U26
SHDN#
GND
IN
SET
OUT
G913C-U
U71
CS4299-XQ
UD1
NC7SZ08-1
U21A
U21C
TSAHCT86
U67
NC7SZ08-1
U58B
TSLCX74-U
-1-24-1
SC-24-2
SC-24-1
AUD_AGND
5V_S0
5VA_S0
3D3V_S0
3D3V_S5
AUDIO_KBC_BEEP#
AUDIO_KBC_BEEP
AUDIO_LDO_SET
AD_XTALIN
AD_XTALOUT
AD_BTCLK
AD_SDIN
AD_BTCLK_F
ADBTCLK
CODEC_EAPD
PCBEEP
PCBEEP_IC
AND_SPKR
AUD_SYS_BEEP
AUD_BEEP1
AUD_BEEP2
MDC_AUDIOIN
PHONE1
LINEINR
LINEINL
MIC
LINE_INR_A
LINE_INL_A
MIC_IN_A
CS_OUT_R_A
CS_OUT_L_A
TB_COVER_SW
KBC_BEEP
14 ICH_AC_BITCLK
21 MDC_BIT_CLK
14,21 ICH_AC_DOUT
14 ICH_AC_DIN0
14,21 ICH_AC_SYNC
14,21 ICH_AC_RST#
19 CB_SPKR
15 ICH_SPKR
21 MOD_AUDIO_IN
17,26 TB_COVER_SW
27 KBC_BEEP
25 CS_OUT_R_A
25 CS_OUT_L_A
25 LINE_INR_A
25 LINE_INL_A
26 MIC_IN_A
12,13,16,17,20,21,23,25,27,28,29,30,31,32,33,36,37,38,39
3,4,7,8,9,12,13,14,15,16,17,18,19,20,21,23,27,28,29,31,32,38,39
26
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC
Size
A3
Document Number
A1+
Rev
-1
Date: Thursday, June 19, 2003
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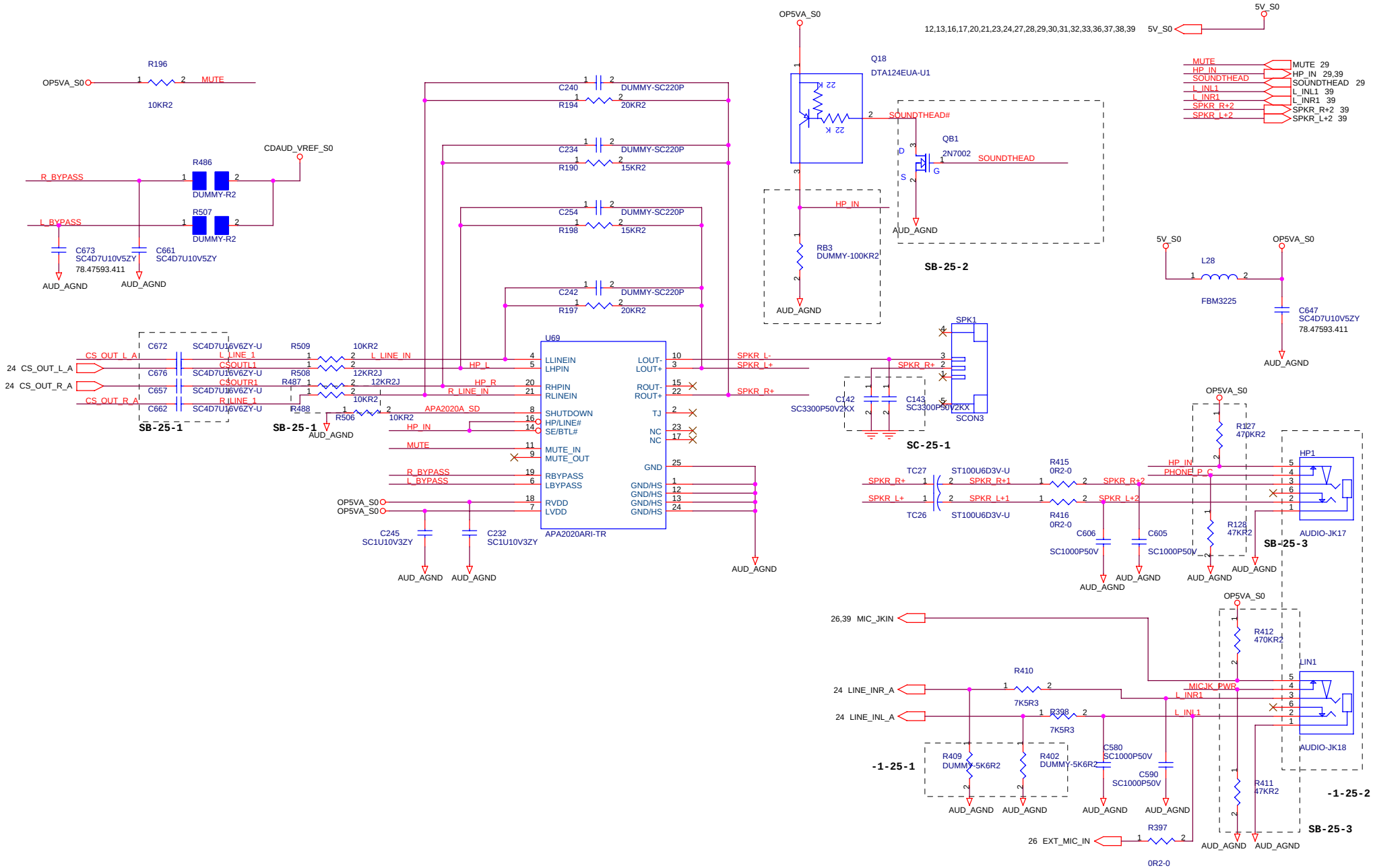

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AUDIO AMP.***	
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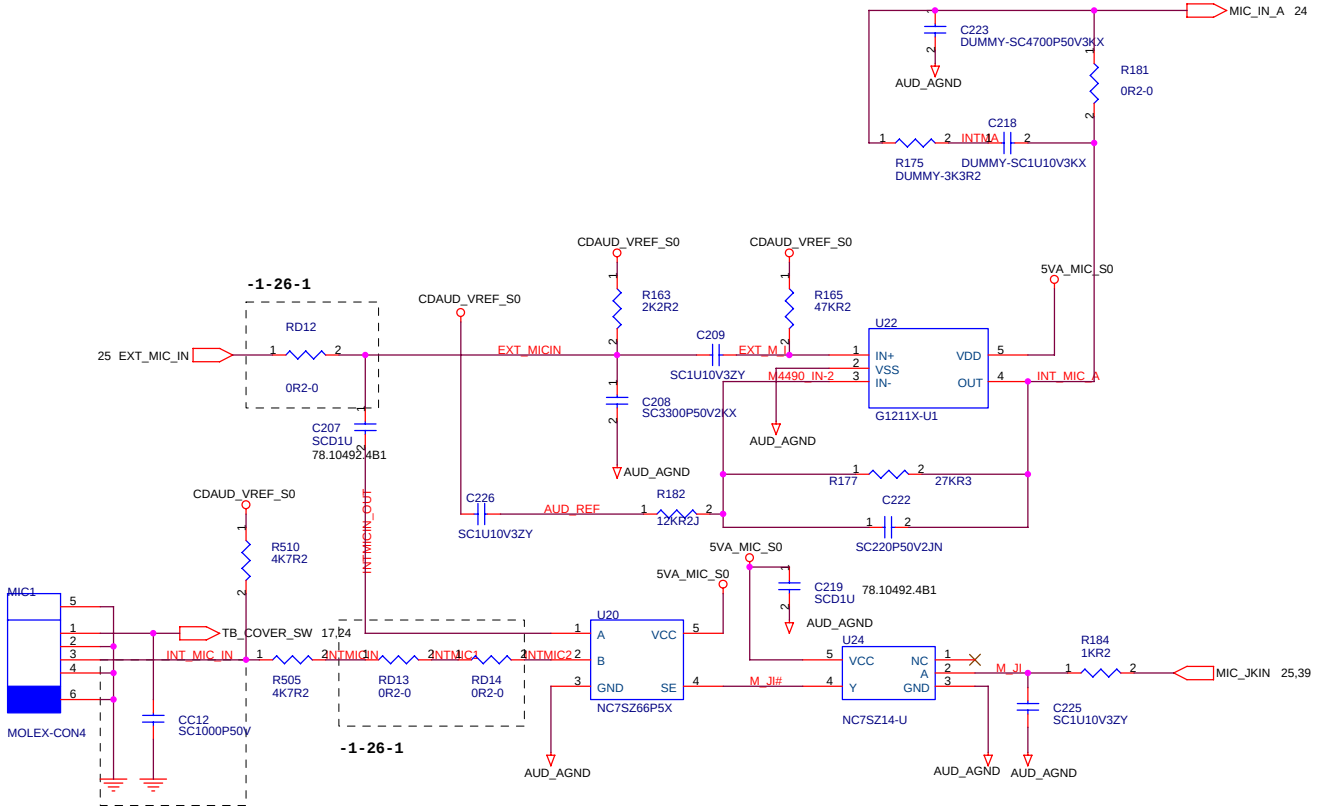
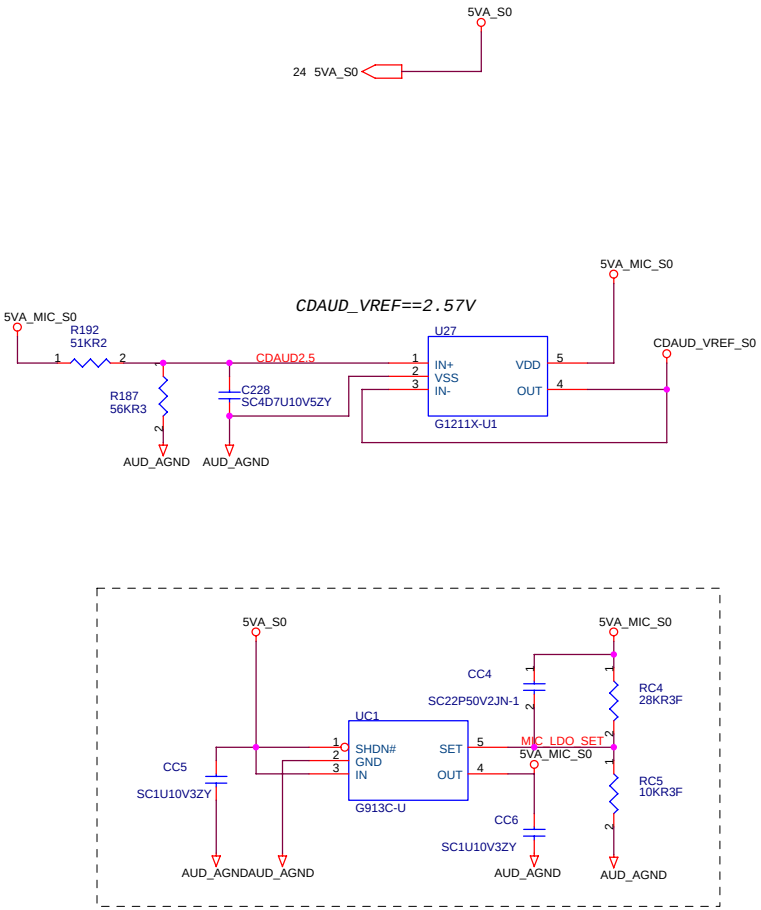


SC-26-2



SC-26-1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MICROPHONE***	
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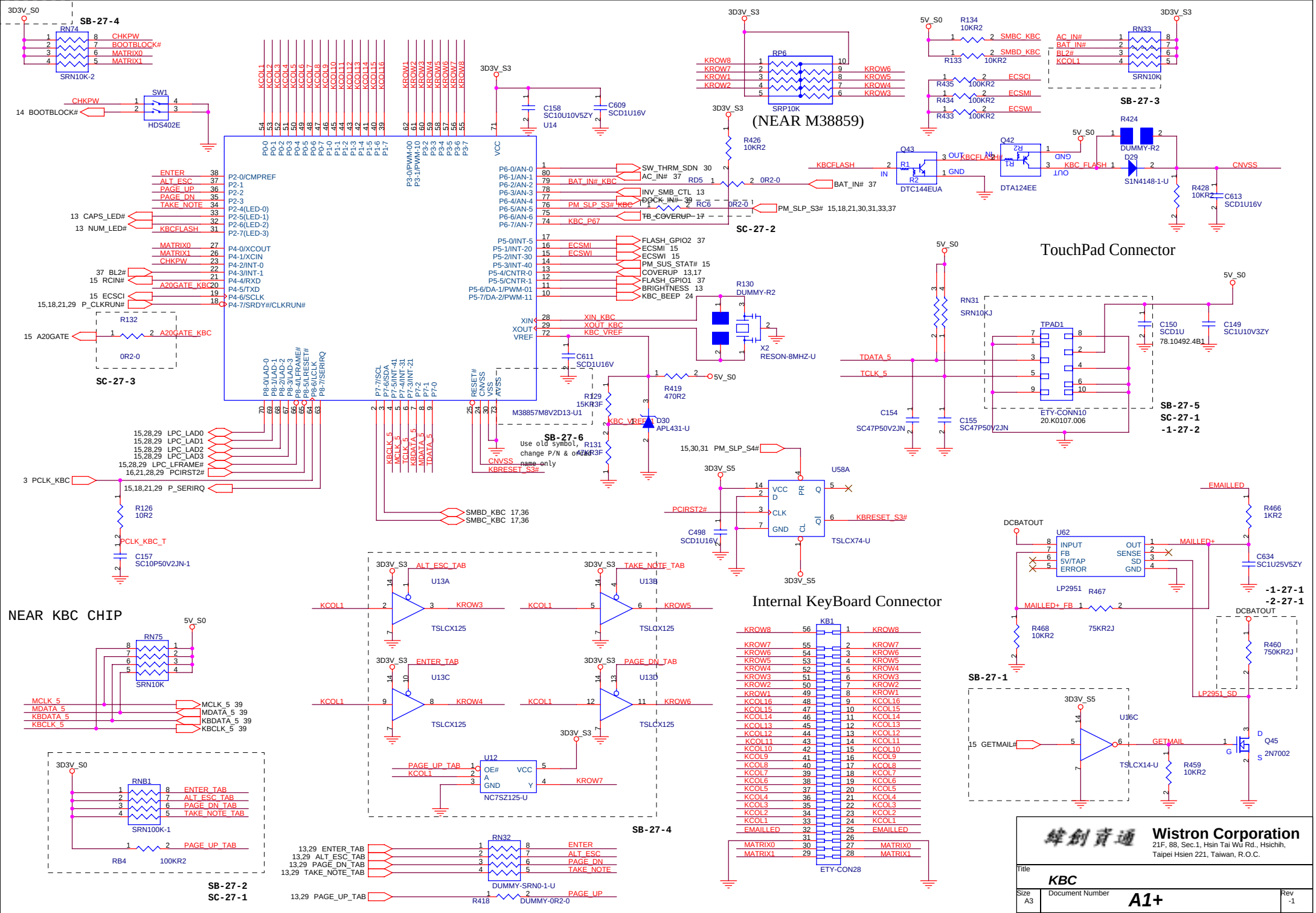
SB-27-4
RN74
SRN10K-2
CHKPW
BOOTBLOCK#
MATRIX0
MATRIX1
SW1
HDS402E
(NEAR M38859)
RP6
SRP10K
RN33
SRN10K
SB-27-3
R134 10KR2
R133 10KR2
R435 100KR2
R434 100KR2
R433 100KR2
ECSCI
ECSMI
ECSWI
R424
DUMMY-R2
D29
S1N4148-1-U
CNVSS
R428 10KR2
C613 SCD1U16V
Q42
DTA124EE
Q43
DTC144EUA
KBCFLASH
BAT_IN# 37
PM_SLP_S3# 15,18,21,30,31,33,37
SC-27-2
TouchPad Connector
RN31
SRN10KJ
TPAD1
ETY-CONN10
20.K0107.006
C150 SCD1U 78.10492.4B1
C149 SC1U10V3ZY
C154 SC47P50V2JN
C155 SC47P50V2JN
TDATA_5
TCLK_5
SB-27-5
SC-27-1
-1-27-2
SC-27-3
R132
0R2-0
A20GATE_KBC
R130 DUMMY-R2
X2 RESON-8MHZ-U
C611 SCD1U16V
R419 470R2
R129 15KR3F
R131 47KR3F
D30 APL431-U
M38857M8V2D13-U1
SB-27-6
Use old symbol, change P/N & only name only
CNVSS
KBRESET_S3#
PM_SLP_S4#
U58A
TSLCX74-U
C498 SCD1U16V
PCIRST2#
KBRESET_S3#
R126 10R2
PCLK_KBC_T
C157 SC10P50V2JN-1
NEAR KBC CHIP
RN75
SRN10K
MCLK_5
MDATA_5
KBDATA_5
KBCLK_5
SMBD_KBC 17,36
SMBC_KBC 17,36
U13A
U13B
U13C
U13D
TSLCX125
ALT_ESC_TAB
TAKE_NOTE_TAB
ENTER_TAB
PAGE_DN_TAB
PAGE_UP_TAB
U12
NC7SZ125-U
RNB1
SRN100K-1
RB4 100KR2
SB-27-2
SC-27-1
RN32
DUMMY-SRN0-1-U
R418 DUMMY-0R2-0
SB-27-4
Internal KeyBoard Connector
KB1
ETY-CON28
EMAILLED
R466 1KR2
C634 SC1U25V5ZY
DCBATOUT
U62
LP2951
R467 75KR2J
MAILLED+
MAILLED+_FB
R468 10KR2
R460 750KR2J
LP2951_SD
-1-27-1
-2-27-1
SB-27-1
U16C
TSLCX14-U
GETMAIL#
GETMAIL
R459 10KR2
Q45 2N7002
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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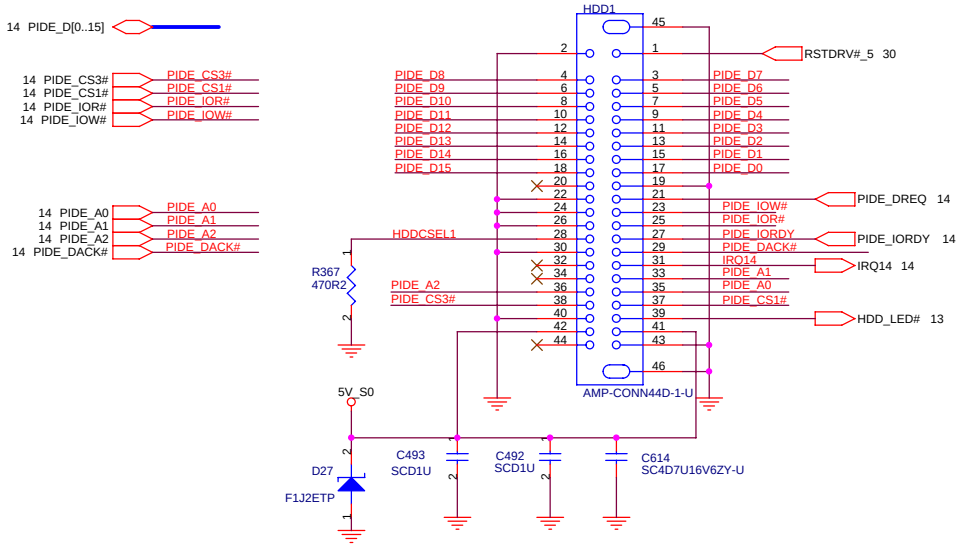
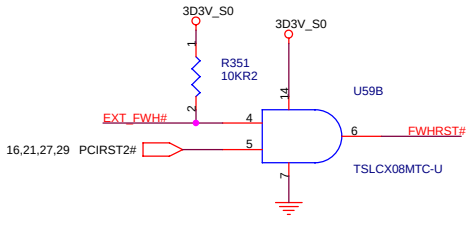
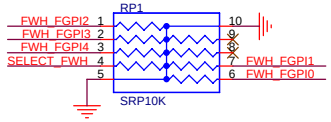
HDD

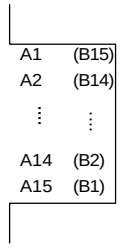




Unused FGPI pins must not be float

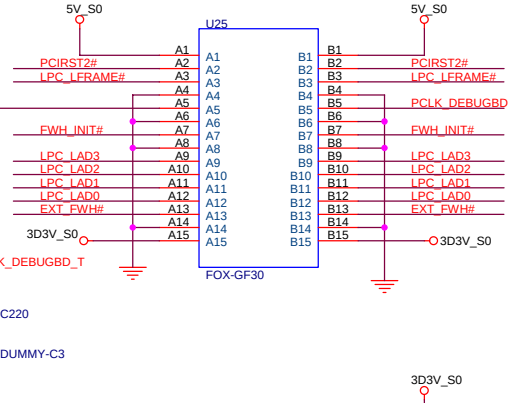


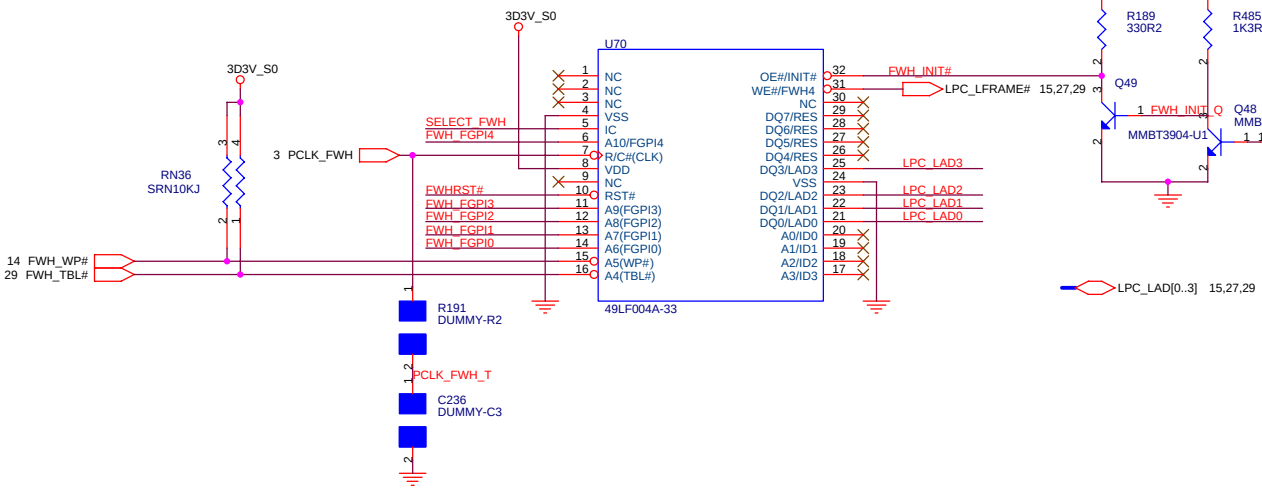
TOP VIEW



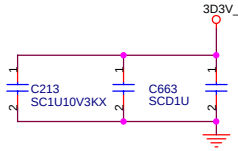
(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD





Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *HDD & FWH & DEBUG*

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A3	*A1+*	-1

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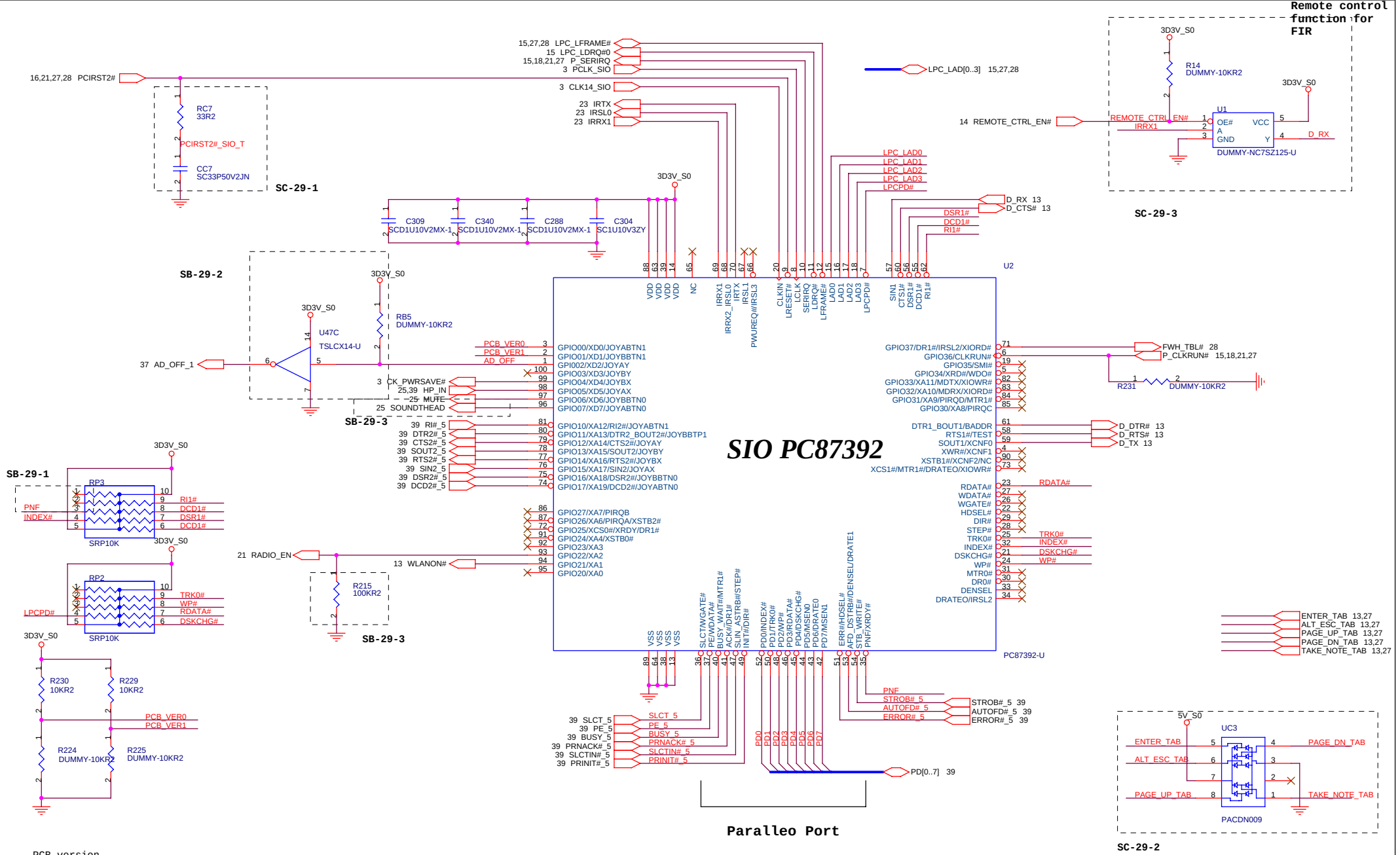

PCB version

PCB_VER0	0	0	1	1
PCB_VER1	0	1	0	1
	SA	SB	SC	-1

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: SIO/FIR

Size: A3 | Document Number: A1+ | Rev: -1

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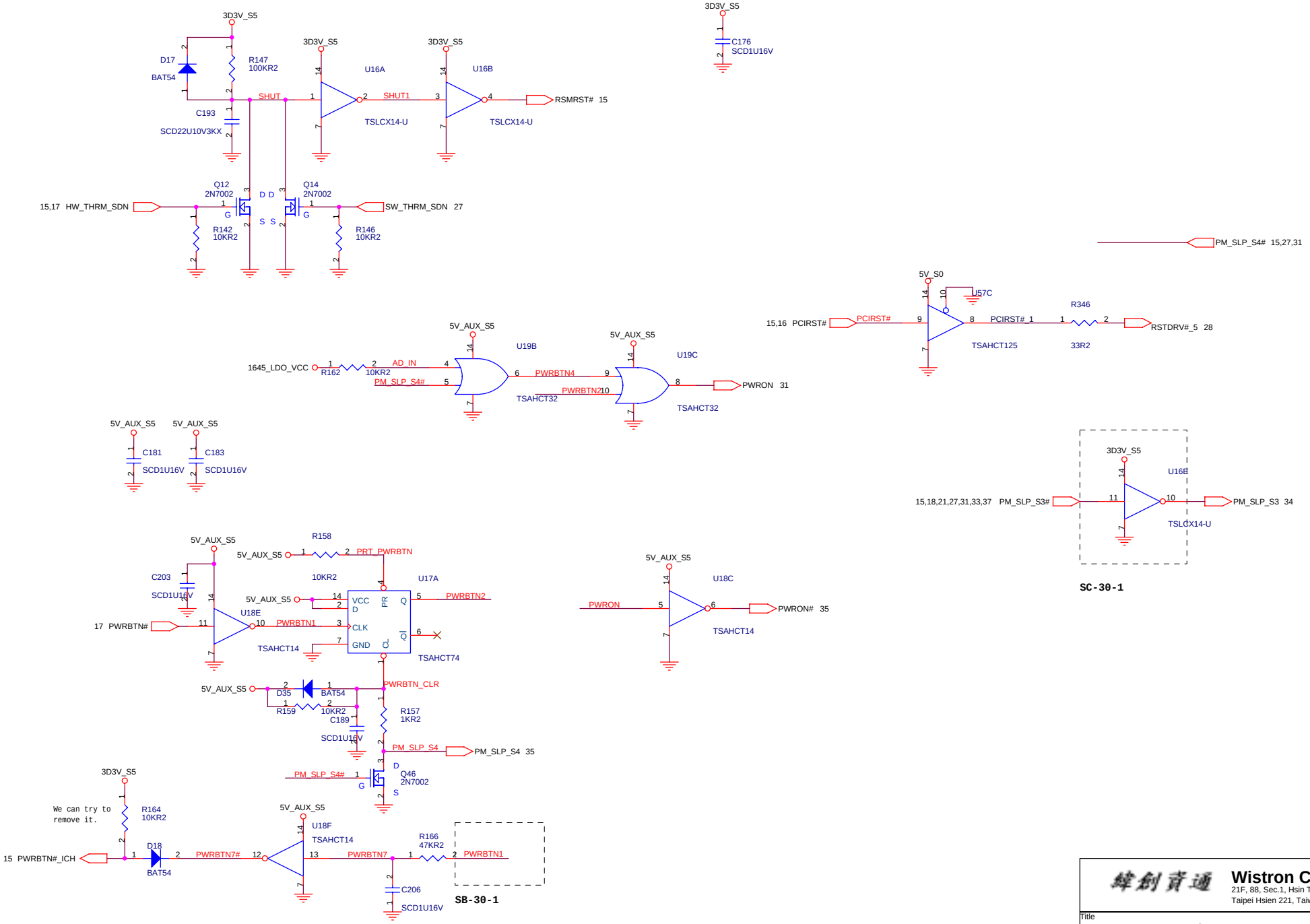
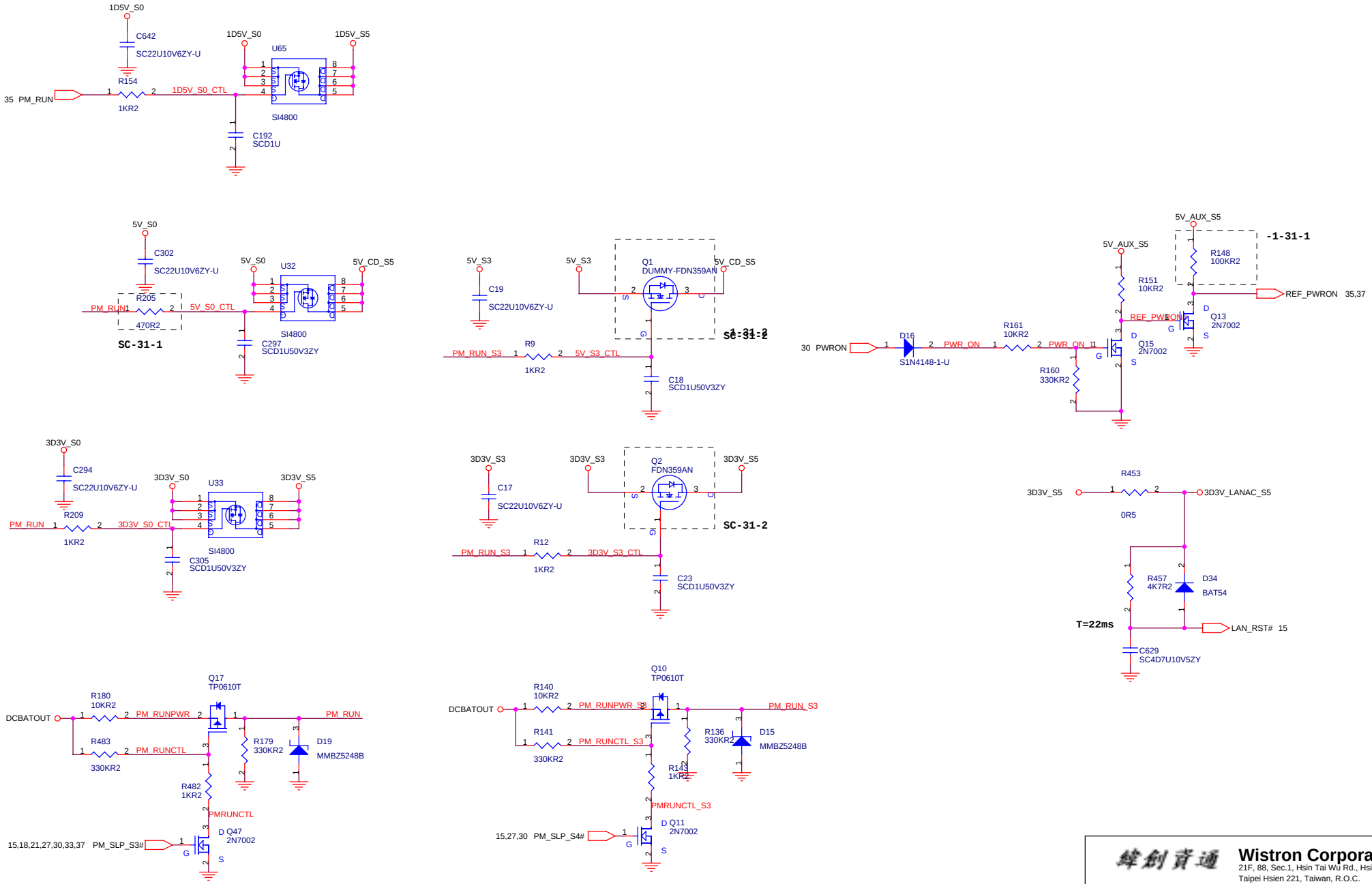


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER ON/RESET LOGIC**

Size: A3 | Document Number: **A1+** | Rev: -1

Date: Thursday, June 19, 2003 | Sheet 30 of 39



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER SWITCH**

Size	Document Number	Rev
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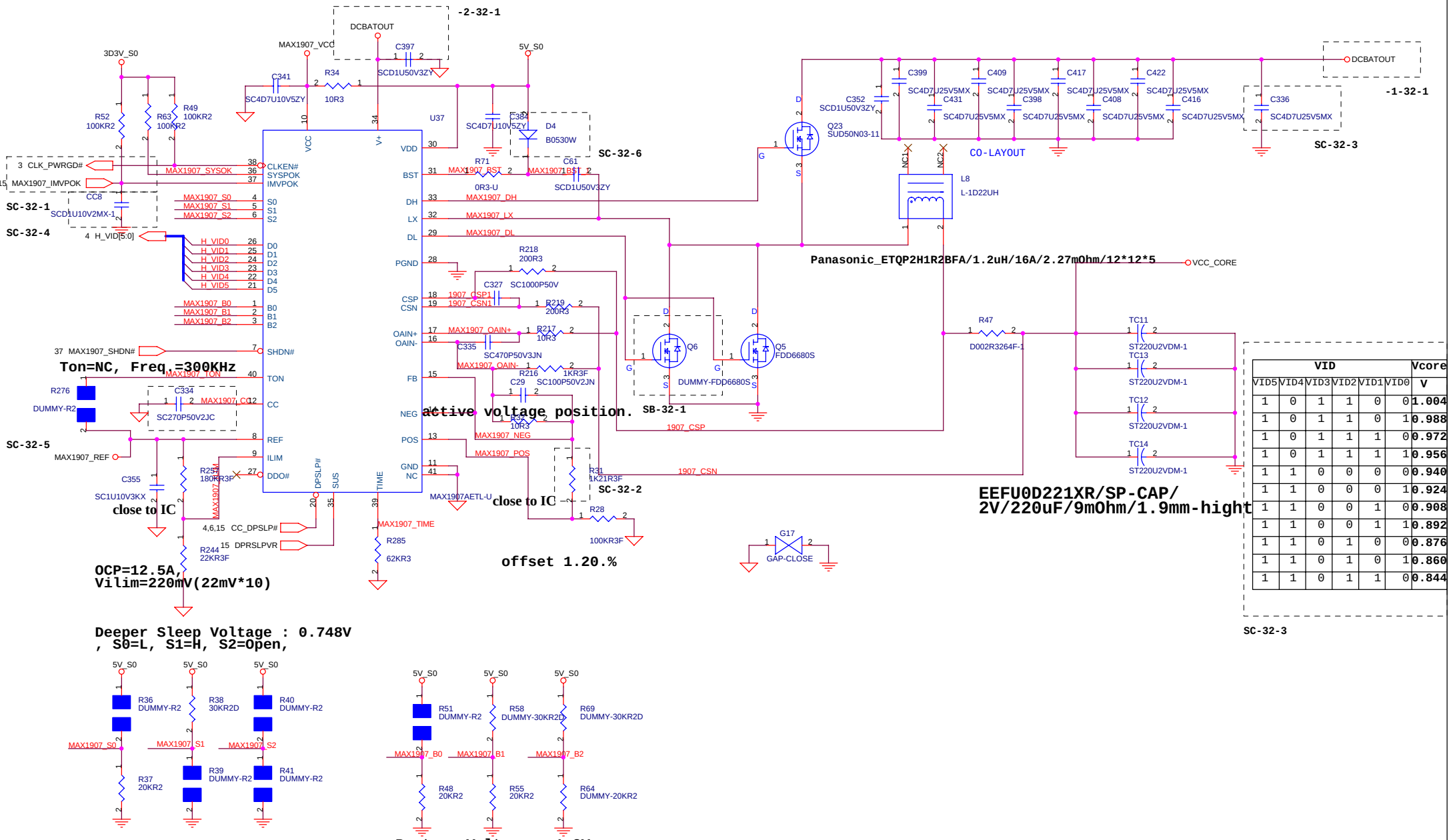

VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
1	0	1	1	0	0	1.004
1	0	1	1	0	1	0.988
1	0	1	1	1	0	0.972
1	0	1	1	1	1	0.956
1	1	0	0	0	0	0.940
1	1	0	0	0	1	0.924
1	1	0	0	1	0	0.908
1	1	0	0	1	1	0.892
1	1	0	1	0	0	0.876
1	1	0	1	0	1	0.860
1	1	0	1	1	0	0.844

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Title: CPU POWER MAX1907

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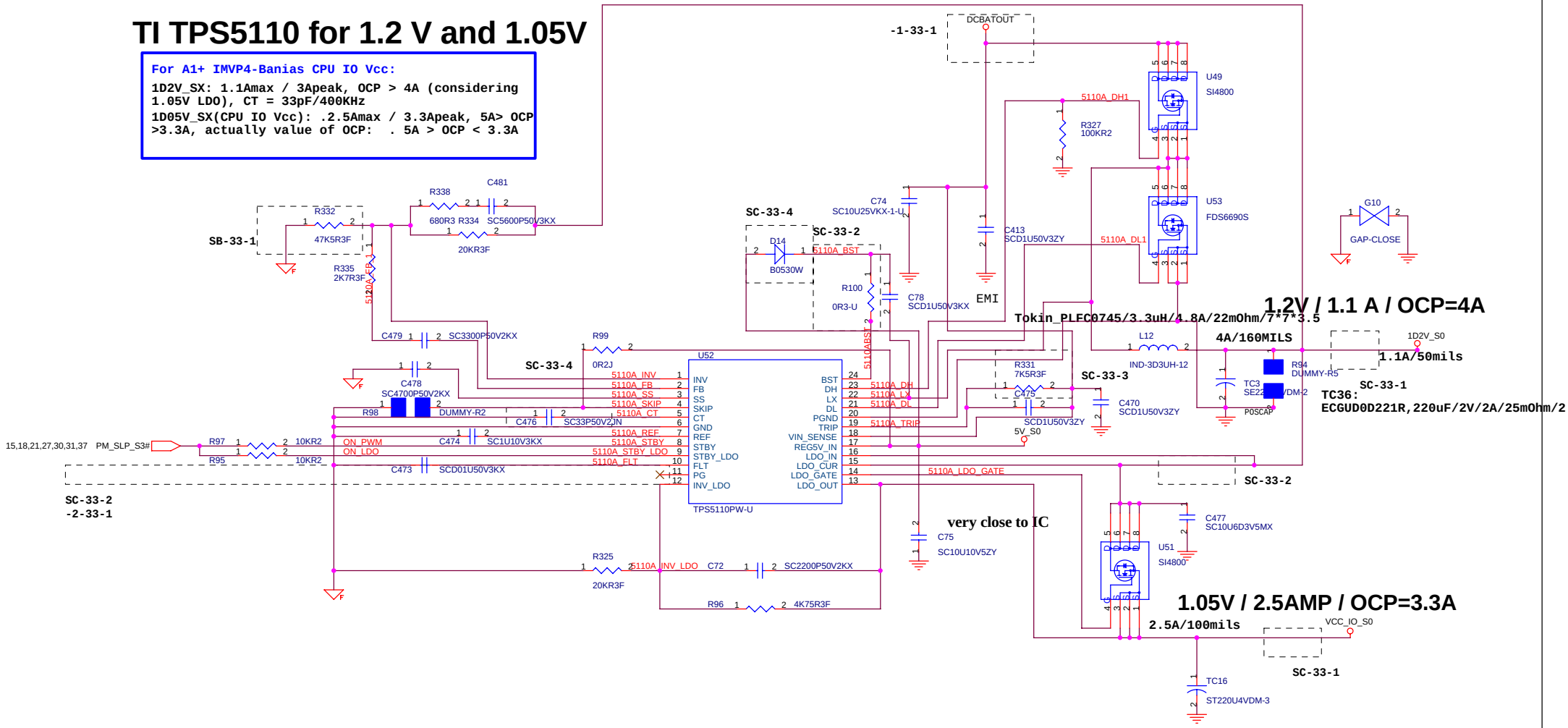
TI TPS5110 for 1.2 V and 1.05V

For A1+ IMVP4-Banias CPU IO Vcc:

1D2V_SX: 1.1Amax / 3Apeak, OCP > 4A (considering 1.05V LDO), CT = 33pF/400KHz

1D05V_SX(CPU IO Vcc): .2.5Amax / 3.3Apeak, 5A> OCP >3.3A, actually value of OCP: . 5A > OCP < 3.3A



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Title	1D2V/1D05V_TPS5110	
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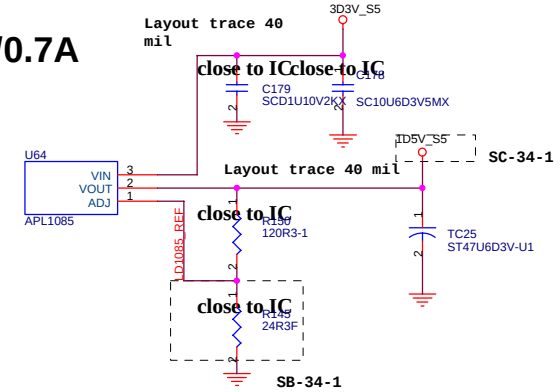
CM8500 & APL1085

APL108574.01085.B3MIC V.R APL1085 3A ADJ T0-252 ANPEC
LD1085CDT-U 74.01085.C3MIC V.R LD1085CDT TO-252ST

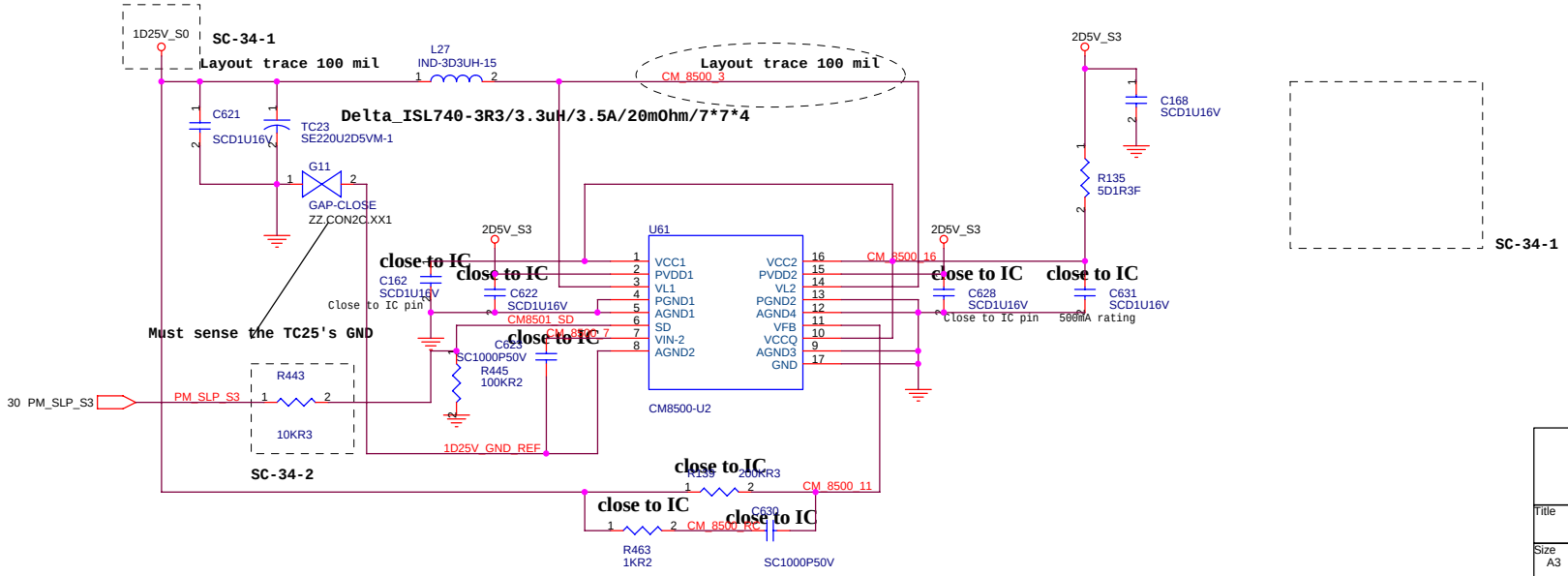
1.5V/0.7A



Vout = Vref * [(Rdown/Rup)+1]
Vref = 1.25V

APL1085 can support 3A, 1.5V/0.7A

CM8500 can support 3A, 1.25V/2.2A



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Title	1D25V/1D5V_CM8500&APL1085	
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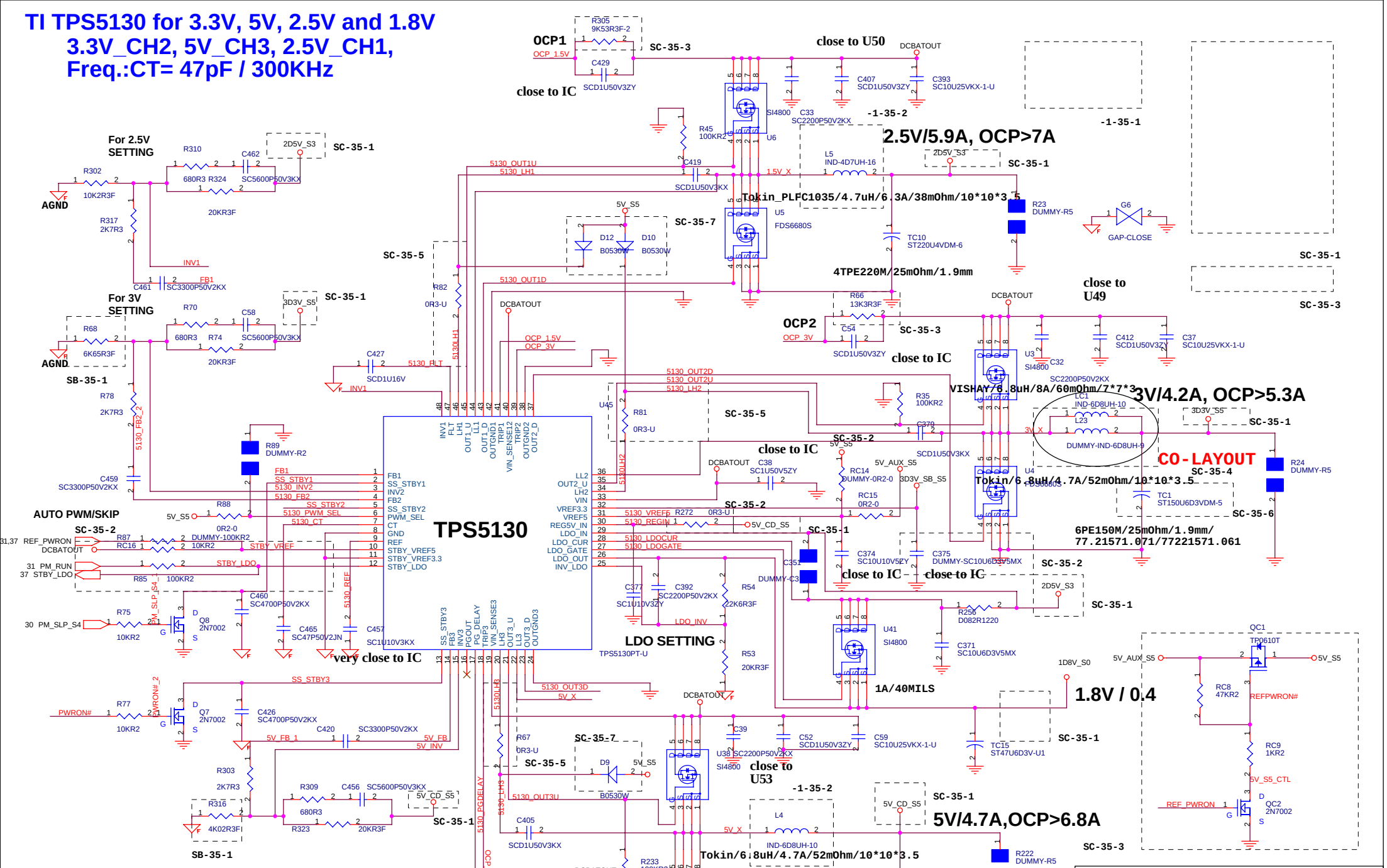
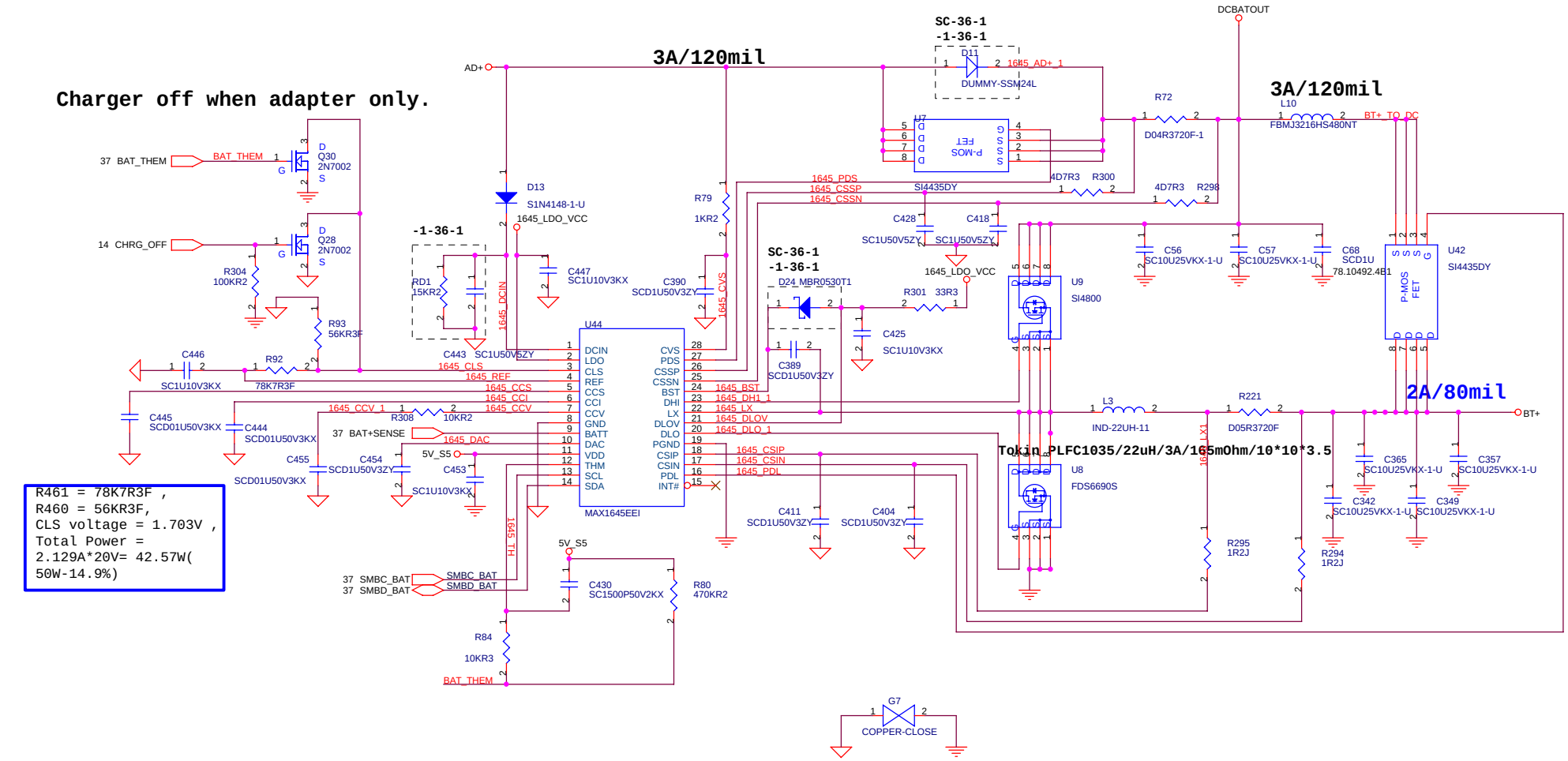
TI TPS5130 for 3.3V, 5V, 2.5V and 1.8V
3.3V_CH2, 5V_CH3, 2.5V_CH1, Freq.:CT= 47pF / 300KHz

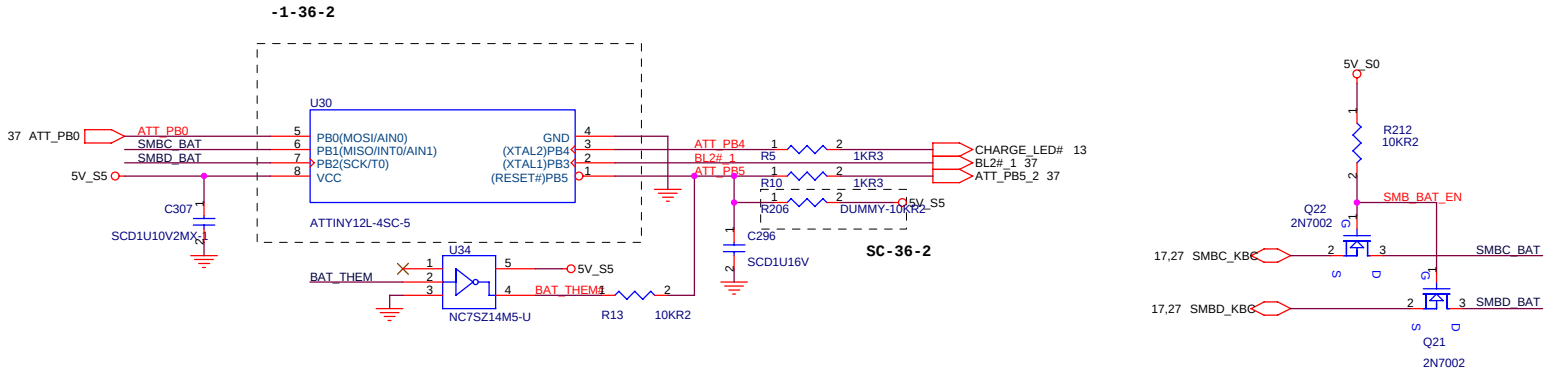


Imax= 50Wpeak = ?Wavg

Charger off when adapter only.



R461 = 78K7R3F ,
R460 = 56KR3F,
CLS voltage = 1.703V ,
Total Power =
2.129A*20V= 42.57W(
50W-14.9%)



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CHARGER MAX1645***	
Size A3	Document Number ***A1+***	Rev -1
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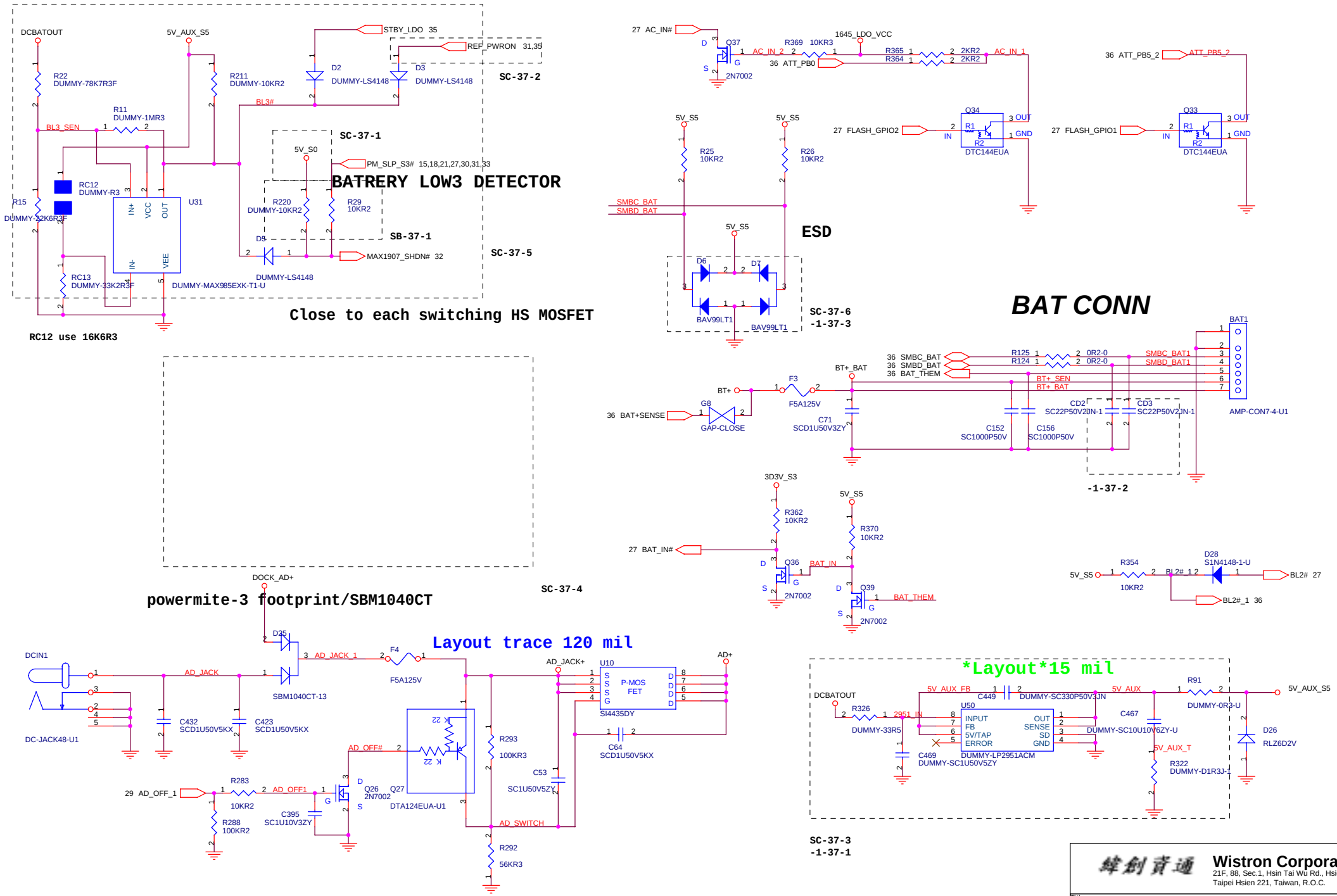

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Title	***BATTERY***	
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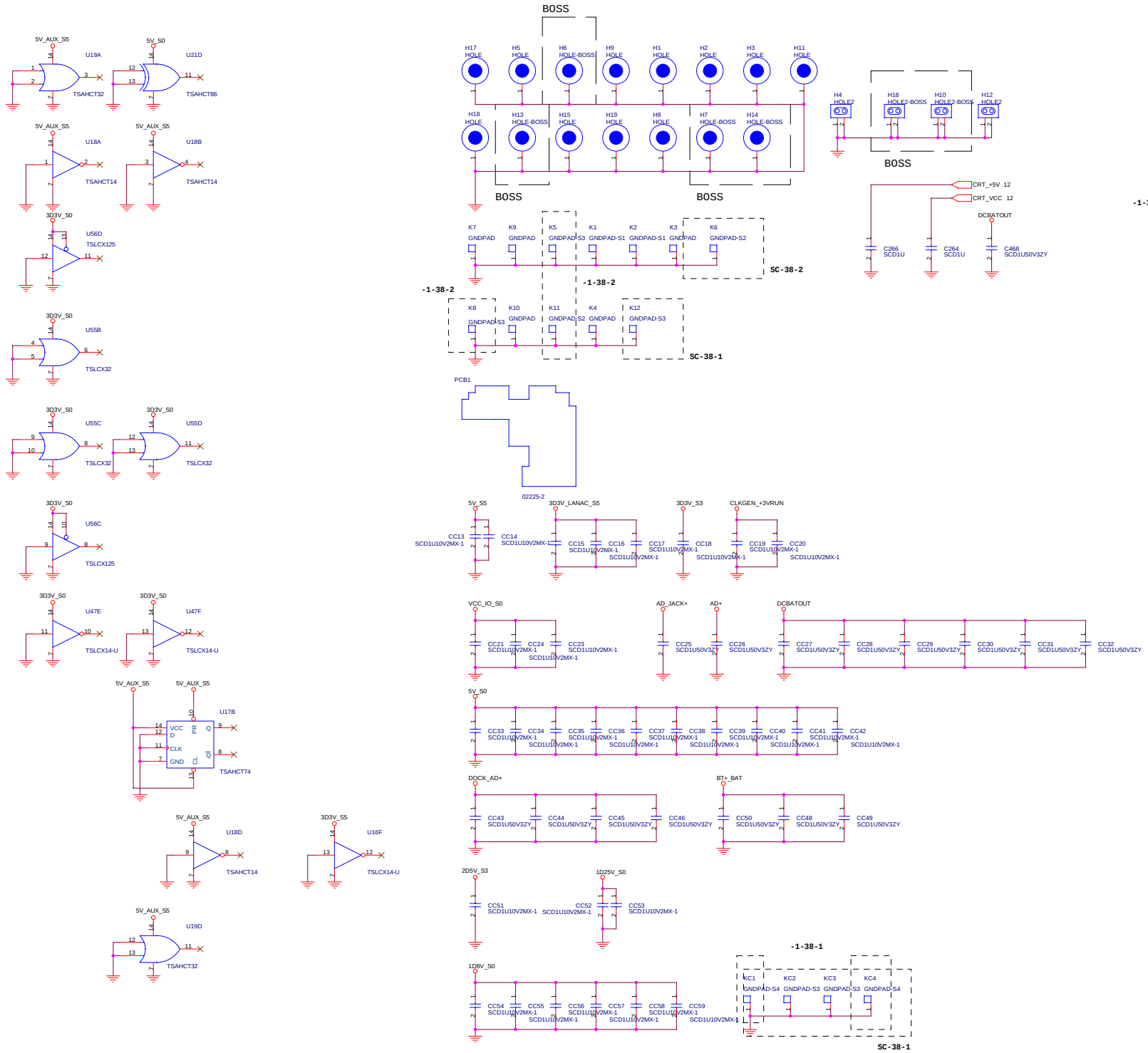

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Title: ***MISC***

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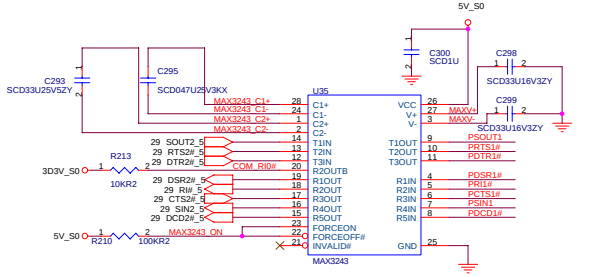
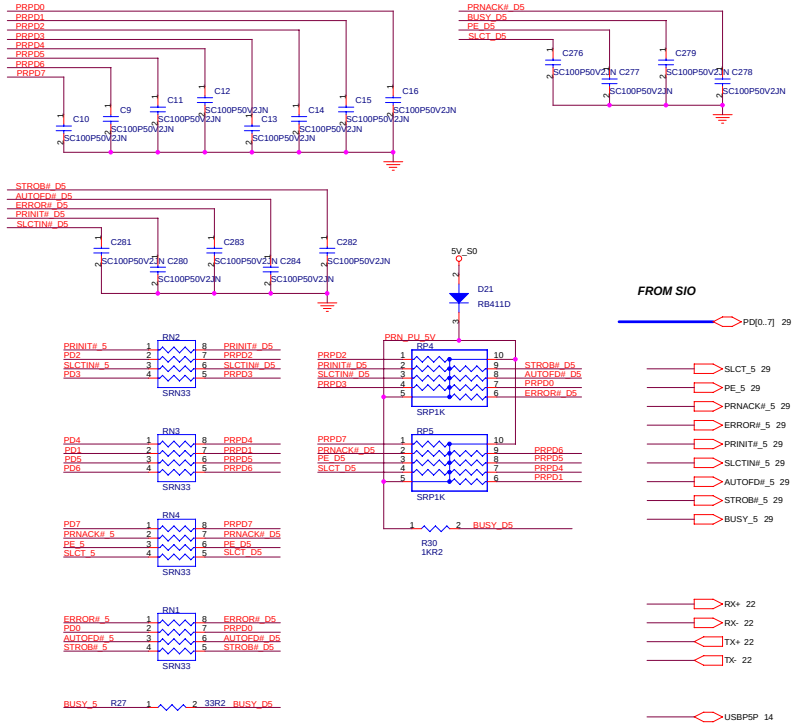
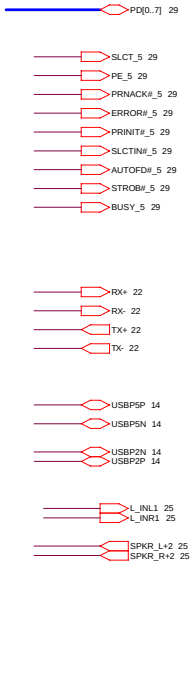
SERIAL PORT

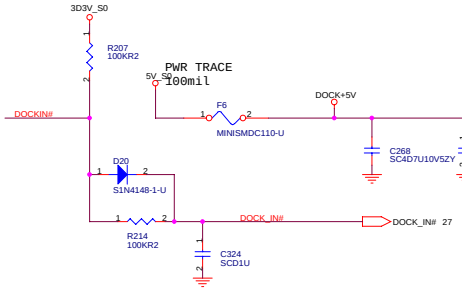


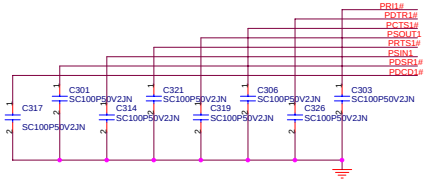
PRINTER PORT

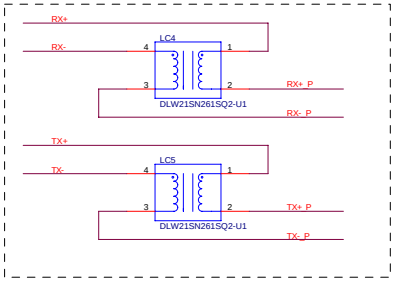


FROM SIO

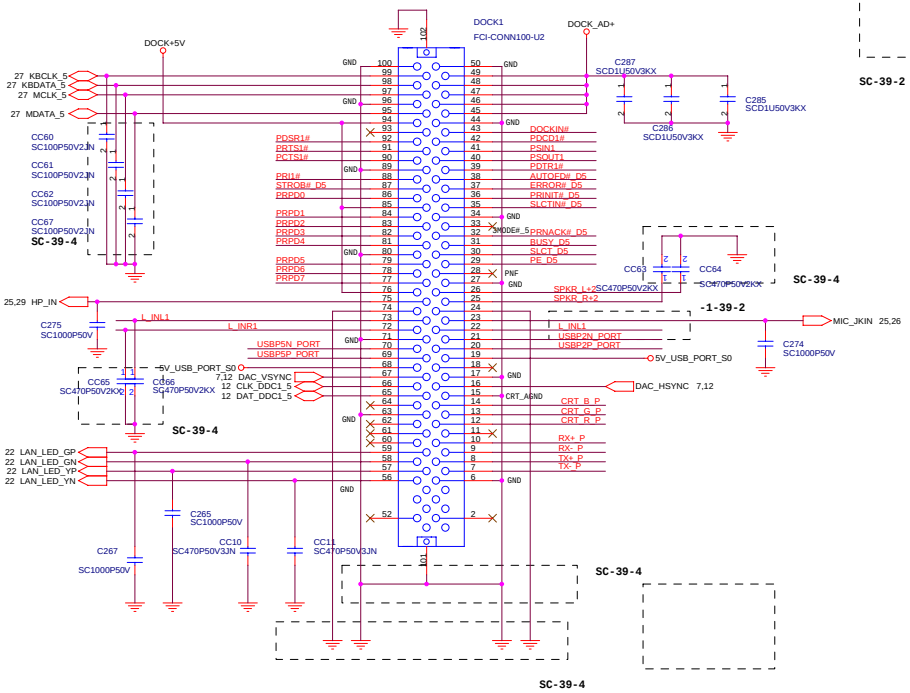




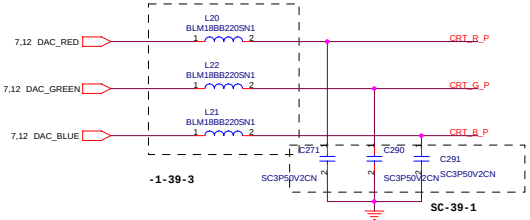


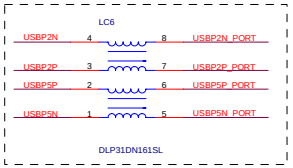


SC-39-2

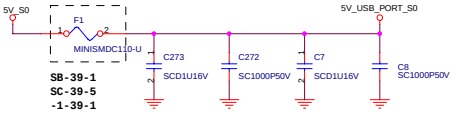


SC-39-4





SC-39-3



SB-39-1
SC-39-5
-1-39-1

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Title: PORT

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